



## Alphawave Semi is accelerating the connected world with complete subsystem interconnectivity IP and I/O and compute chiplet solutions

Alphawave Semi design industry-leading, high-speed connectivity solutions for customers in high-growth end markets including Data Center, AI, 5G wireless infrastructure, Data networking and Solid-state storage. Our leading-edge technology advances push the boundaries of wired connectivity capabilities, enabling data to travel faster, more reliably, and using lower power.

### ZeusCORE™ MSS IP Supporting Linear Pluggable Optics

The Alphawave Semi ZeusCORE™ is a Xtra-Long-Reach (XLR, LR, MR, VSR), DSP-based, Multi-Standard SerDes (MSS) IP. It is a highly configurable SerDes IP that supports all leading edge NRZ and PAM4 data center standards from 1Gbps to 112Gbps, optimized for up to 43 dB bump-bump lossy channel. This IP is proven in silicon in leading edge process nodes (7nm, 6nm, 5nm, 4nm, 3nm) and ready for customer tape outs.

#### Key Features:

- Support diverse protocols such as PCI-Express® 1.0 to 6.0 and 1G/10G/25G/50G/100Gbps Ethernet
- Maximum Likelihood Sequence Detector (MLSD) enables extra-long channels.
- Can extend raw BER by 2+ orders of magnitude for channels operating at high error rates

### OmegaCORE™ 1.6T Multi-protocol Controller

The OmegaCORE™ 1.6T Multi-protocol Controller from Alphawave IP is a multi-channel, multi-rate Ethernet aggregator that supports tributaries from 10GE to 800GE, utilizing the 112G/s, 56G/s, and 28G/s SerDes. The Core consists of Multi-channel and Multi-rate PCS and MAC Cores. The supported Ethernet protocols are 10G, 25G, 40G, 50G, 100G, 200G, 400G, 800G. With Core clock frequency of 800MHz to 1.6GHz at TSMC 7nm, 5nm and 3nm, this Core delivers smallest footprint among similar solution in the Ethernet/Fiberchannel/FlexO SOC market.

#### Key Features:

- Digital Crossbar among all SerDes lanes in both TX and RX direction in the SerDes Mux/Demux
- Supports IEEE 802.3 required FEC variants
- Standard ETC 800GE supports with bonded 2 x 400GE PCS and a single 800G MAC

Provides OTN, FlexE, FlexO, OTU25/50-RS, xGFC access ports (Optional add-on)



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## AlphaCHIP1600-I/O Supporting Linear Pluggable Optics

The Alphawave Semi AlphaCHIP1600-IO™ chiplet contains an Xtra-Long-Reach (XLR, LR, MR, VSR), DSP-based, Multi-Standard SerDes (MSS) IP. It is a highly configurable SerDes IP that supports all leading edge NRZ and PAM4 data center standards from 1Gbps to 112Gbps, optimized for up to 43 dB bump-bump lossy channel. This chiplet has PCIe, CXL, and Ethernet configurations that can be connected to a main die over a UCIe.

### Key Features:

- Create cost-effective high-availability hyperscale systems by enabling scale-up SoC via UCIe Interconnect
- Simplify connectivity while providing the highest Ethernet and PCIe performance available for data center servers, AI, storage, and networking
- Exploit the benefits of silicon-proven Interconnect IP to accelerate the next generations of semiconductors
- Reduce latency, system complexity, and power consumption by up to 50% in data-intensive environments

## AlphaCHIP32-C: An Energy Efficient Arm Neoverse Compute Chiplet

AlphaCHIP32-N3C is a high-performance, low-power, compute chiplet with support for industry standard interfaces such as PCIe, CXL, UCIe, and AMBA CHI C2C. It enables customers with Arm's high performance Neoverse compute cores. World leading, low power, DSP-based SerDes technology provides monolithic connectivity to the accelerator over CHI-C2C. Industry leading UCIe offers a die-to-die link to an accelerator chiplet or an I/O chiplet that can easily be integrated into any multi-die packaging solution.

### Key Features:

- Enables customers to focus on accelerator design with the use of off-the-shelf compute connectivity
- Delivers high energy efficiency CPU compute power with high performance per-watt and low latency
- Create cost-effective high-availability hyperscale systems by enabling scale-up SOC via UCIe Interconnect
- Exploit the benefits of silicon-proven Interconnect IP to accelerate the next generations of semiconductors

