ALPHAWAVE SEMI

Alphawave Semi is accelerating the connected world with complete subsystem interconnectivity IP and custom compute solutions

Alphawave Semi design industry-leading, high-speed connectivity solutions for customers in high-growth end markets including Data Center, AI, 5G wireless infrastructure, Data networking, Autonomous vehicles and Solid-state storage. Our leading-edge technology advances push the boundaries of wired connectivity capabilities, enabling data to travel faster, more reliably, and using lower power.

ZeusCORE™ MSS IP Supporting Linear Pluggable Optics

The Alphawave Semi ZeusCORE™ is a Xtra-Long-Reach (XLR, LR, MR, VSR), DSP-based, Multi-Standard SerDes (MSS) IP. It is a highly configurable SerDes IP that supports all leading edge NRZ and PAM4 data center standards from 1Gbps to 112Gbps, optimized for up to 43 dB bump-bump lossy channel. This IP is proven in silicon in leading edge process nodes (7nm, 6nm, 5nm, 4nm, 3nm) and ready for customer tape outs.

Key Features:

- Support diverse protocols such as PCI-Express® 1.0 to 6.0 and 1G/10G/25G/50G/100Gbps Ethernet
- Maximum Likehood Sequence Detector (MLSD) enables extra-long channels.
- Can extend raw BER by 2+ orders of magnitude for channels operating at high error rates

OmegaCORE™ 1.6T Multi-protocol Controller

The OmegaCORE™ 1.6T Multi-protocol Controller from Alphawave IP is a multi-channel, multi-rate Ethernet aggregator that supports tributaries from 10GE to 800GE, utilizing the 112G/s, 56G/s, and 28G/s SerDes. The Core consists of Multi-channel and Multi-rate PCS and MAC Cores. The supported Ethernet protocols are 10G, 25G, 40G, 50G, 100G, 200G, 400G, 800G. With Core clock frequency of 800MHz to 1.6GHz at TSMC 7nm, 5nm and 3nm, this Core delivers smallest footprint among similar solution in the Ethernet/Fiberchannel/FlexO SOC market.

Key Features:

- Digital Crossbar among all SerDes lanes in both TX and RX direction in the SerDes Mux/Demux
- Supports IEEE 802.3 required FEC variants
- Standard ETC 800GE supports with bonded 2 x 400GE PCS and a single 800G MAC
- Provides OTN, FlexE, FlexO, OTU25/50-RS, xGFC access ports (Optional add-on)

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PipeCORE™ PCIe 7.0 Subsystem IP Supporting Optical PCIe

The Alphawave PipeCORE Subsystem IP is a high-performance, low-power, PCIe 1.0 to PCIe 7.0 PHY with integrated Alphawave Semi's controller IP delivering a complete subsystem supporting up to PCIe 6.0 or CXL 3.1.

Key Features:

- Low Power Architecture on the Integrator's List
- Targeted for 30+ dB of channel loss for PCIe Gen1 to Gen7 and CXL NRZ and PAM4
- Passes Gen6 JTOL

AresCORE™ UCIe Subsystem IP Supporting Energy Efficient Interfaces

AresCORE is a silicon-proven, market leading extremely low-power, low-latency Universal Chiplet Interconnect Express (UCIe™) Die-to-Die PHY IP designed by Alphawave Semi for very high bandwidth connections between two dies that are on the same package.

Key Features:

- Alphawave Semi's Complete UCIe Solution for an open and robust chiplet ecosystem
- Optimized for high-bandwidth density – Up to 36Gbps data-rate-per-lane, low-power, low-latency multi-module PHY and leverages silicon-proven analog IPs
- The AresCORE PHY IP can be configured to support advanced packaging such as Silicon Interposer, RDL Interposer, Integrated Fan-Out and Silicon Bridge for maximum density, and organic substrates for the most cost-effective solution covering all market segments
- The AresCORE PHY IP is available in leading-edge foundries across multiple technology nodes

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