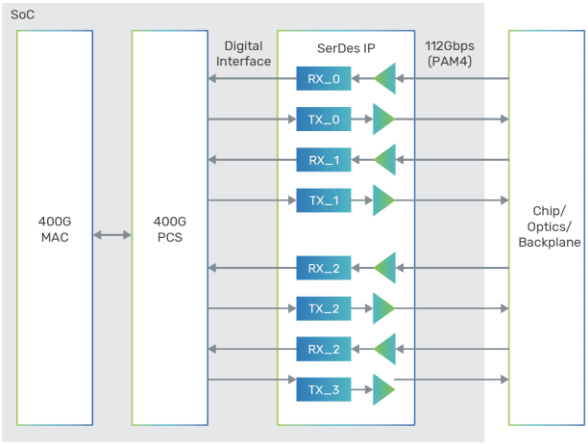
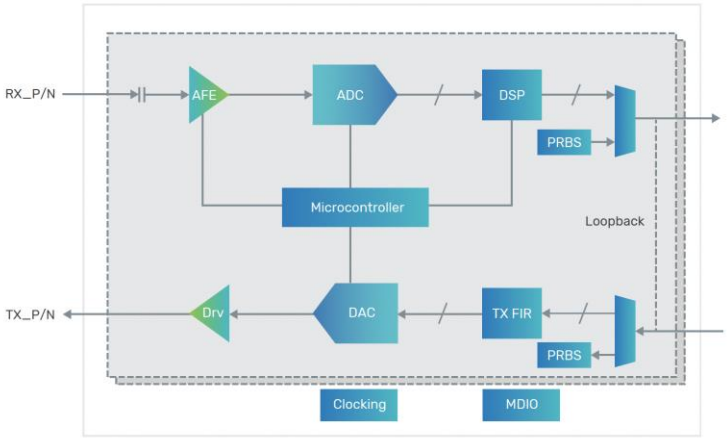
Cadence Design Systems, Inc.

At OFC 2023, Cadence is participating in demonstrations showcasing CEI-112G-LR interoperability.

Cadence 112G Long-Reach (LR) SerDes PHY IP enables reliable high-speed data transfer over backplane, direct-attached cable (DAC), chip-to-chip, and chip-to-module channels for cloud networking, artificial intelligence and machine learning (AI/ML), and 5G wireless applications. With extended long-reach capability, it supports NRZ and PAM4 signaling from 1Gbps to 112Gbps for LR/MR/VSR channels with additional performance margin. The IP incorporates analog-to-digital converter (ADC), clock-data-recovery (CDR), and digital signal process (DSP) technology. It can support up to 800G Ethernet with IP subsystems including PCS and MAC available. Learn more at https://www.cadence.com/go/112g.



Example system-level block diagram



IP-level block diagram

CEI-112G-LR Interoperability: Cadence and other OIF members are demonstrating various aspects of CEI-112G-LR interoperability. Cadence's 112G-LR SerDes PHY is used to receive signals from the transmitter of another vendor's SerDes through an LR channel that is provided by multiple vendors.

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