SYNOPSYS®

224G Ethernet PHY IP

Highlights

- Supports full-duplex 1.25 to 224Gbps data rates
- Enables 200G, 400G, 800G, and 1.6T Ethernet
- Ethernet interconnects for wired network infrastructure
- Supports IEEE 802.3 and OIF-224G standards electrical specifications
- Meets the performance requirements of chip-to-chip, chip-to-module, and long reach copper/backplane interconnects
- DAC-based PAM-4/6 transmitter includes feed-forward equalization (FFE)
- Digital-based receiver consists of analog front-end (AFE), ADC, and advanced digital signal processor (DSP)
- High-performance receiver equalization supports channel loss of 45dB
- Continuous calibration and adaptation (CCA) provides robust performance across voltage, and temperature
- Low jitter phase-locked loops (PLLs) provide robust timing recovery and better jitter performance

Target Applications

- Hyperscale data center
- Enterprise and campus networks
- High-performance computing/networking
- Service provider networks
- Artificial intelligence and machine learning

Technology

3-nm FinFET process

Overview

The Synopsys 224G Ethernet PHY IP, an integral part of Synopsys' high-speed SerDes IP portfolio, meets the growing high bandwidth and low latency needs of high-performance data center applications. Using leading-edge design, analysis, simulation, and measurement techniques, the Synopsys 224G Ethernet PHY delivers exceptional signal integrity and jitter performance that supports the IEEE 802.3 and OIF standards electrical specifications. The PHY is small in area and high in performance, demonstrating zero post-FEC BER.

The PHY supports the Pulse-Amplitude Modulation 4/6-Level (PAM-4/6) and Non-Return-to-Zero (NRZ) signaling to deliver up to 1.6T Ethernet. The configurable transmitter and advanced DSP-based receiver with analog-to-digital converter (ADC) enable designers to control and optimize signal integrity and performance. The CCA algorithm provides a robust performance across voltage and temperature variations. The low jitter PLLs and multi-loop clock and data recovery circuits provide robust timing recovery and better jitter performance, while the embedded bit error rate (BER) tester and internal eye monitor provide on-chip testability and visibility into channel performance.

The PHY has been co-designed and optimized with the Synopsys Physical Coding Sublayer (PCS) and Media Access Controller (MAC) IP to reduce integration time and provide solution level differentiation.

Combined with Synopsys' routing feasibility study, packages substrate guidelines, signal and power integrity models, and thorough crosstalk analysis, Synopsys provides a comprehensive 224G Ethernet PHY solution for fast and reliable SoC integration and first pass silicon success.

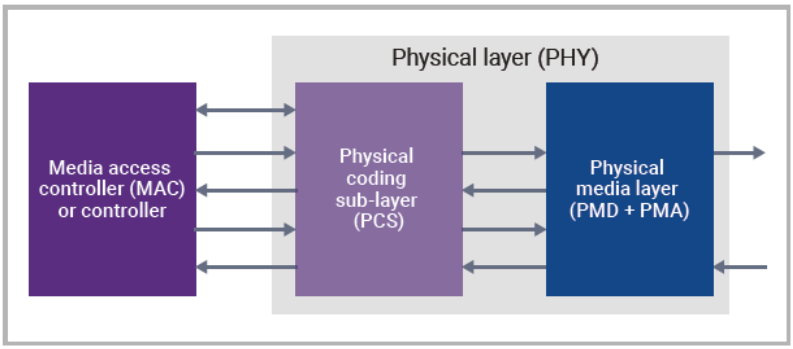

Figure 1. Synopsys 224G Ethernet PHY IP

OIF PLL INTEROP DEMO
ECOC 2023
www.oiforum.com

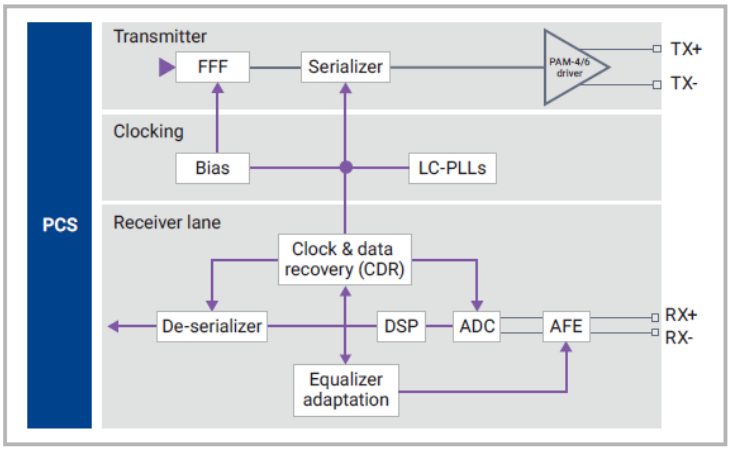

Figure 2. Synopsys 224G Ethernet IP block diagram

Key Features

- Optimized for performance, power, and area
- Includes one, two, or four full-duplex PAM-4/6 transceivers (transmit and receive functions)
- Supports IEEE and OIF-CEI-224G standards
- Includes auto-negotiation and link training capabilities
- Low jitter transmitter and receiver (dual loop clock and data recovery) clock architectures
- Multi-lane PHY shares a single clock and support core
- Supports both internal and external reference clock connections to the PHY
- Configurable transmitter and advanced DSP-based receiver with analog-to-digital converter
- Optimal receiver jitter tolerance supports a wider range of board layout designs and immunity to interference (cross talk), and reduces design constraints on board signal paths
- Contains embedded pseudo random bit sequence (PRBS) for internal and external loopbacks
- Embedded bit error rate (BER) tester and non-destructive internal eye monitor

Deliverables

- Verilog models and test bench; Protocol-specific test bench; Liberty timing views (.lib), LEF abstracts (.lef), CDL netlist (.cdl); GDSII; IP-XACT XML files with register details; ATPG models; IBIS-AMI models; Documentation

About Synopsys IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad Synopsys IP portfolio includes logic libraries, embedded memories, PVT sensors, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits, and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market.

For more information on Synopsys IP, visit synopsys.com/ip .