TDM System Interface Protocol (TDM-P) Implementation Agreement

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ABSTRACT: Implementation Agreement for a TDM System Interface Protocol (TDM-P), which multiplexes either 2 or 4 TFI-5 signals into a doubled or quadrupled speed signal, respectively, based on the Common Electrical Interface (CEI).

OPTICAL INTERNETWORKING FORUM

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4 Document Revision History

Revision	Date	Description
OIF-TDM-P-01.1	April 2006	IA Text derived from Draft IA text of document oif2005.311.00 accepted by OIF principal ballot #43

5 Introduction

At the January 2005 OIF Plenary meeting, the project was approved to generate an Implementation Agreement called TDM-P (TDM System Interface Protocol).
TDM-P shall provide a protocol for aggregation of TFI-5 signals, like specified in [1], with optimized implementation effort (gate count) and scalability of link speed (1x, 2x or 4x) on a per link basis.
The electrical specification for this protocol shall be according to OIF-CEI [2].

6 Requirements

It is desirable for the protocol to comply with the following objectives and requirements:

- TDM-P will define a data protocol for multiplexing 2 or 4 TFI-5 signals into CEI 6G and 11G signal rates (1)
- The interface shall be point-to-point
- Transmitter and receiver are fully synchronous, e.g. no rate adaptation
- Signal rate shall be factor 2.0 or 4.0 of TFI-5 rate
- The protocol shall be applicable for links, where FEC is not required to reach the BER of interest
- It shall be easy to implement with high re-use and multi-use of TFI-5 macro functions
- It shall support easy switching between legacy TFI-5 mode and factor 2 or 4 TFI-5 rates on a per link basis
- It shall be optimized for implementation effort in devices with a high number of CEI links
- Predictable connection of aggregated TFI-5 ports shall be maintained at any time by the protocol
- It shall enable use of existing test and measurement equipment for analysis of the signal

Note (1): TFI-5 signals of 2.488 Gbps will be mapped into 4.976 Gbps or 9.952Gb/s. TFI-5 signals of 3.11 Gbps will be mapped into 6.2208 Gbps, factor 4 for this signal type will not be covered as out of scope for OIF-CEI [2]

This Agreement will not:

- Define the electrical specification as this is defined by CEI
- Define any optical specification

7 Interface Definition

TDM-P is a SONET/SDH-like backplane interface protocol, aggregating multiple TFI-5 [1] signals into higher rates (x2, x4), like specified in OIF-CEI [2]. The electrical specification is according to OIF-CEI [2].
Figure 1 shows the System Reference Model for TDM-P. According to the data bandwidth need, there can be as many TDMPDATA links as required to transport it between the two devices.

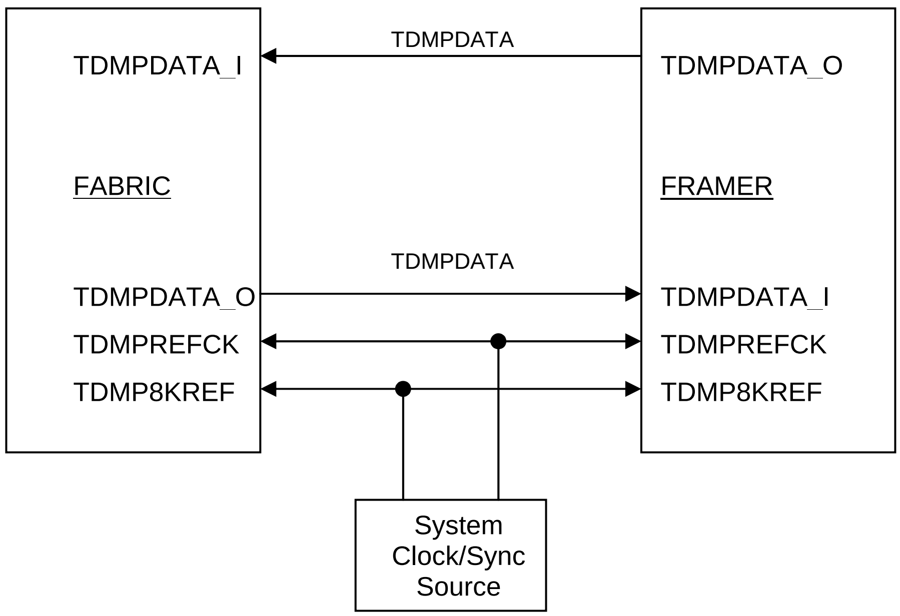

Figure 1: TDM-P System Reference Model

Similar to TFI-5 the services provided by the TDM-P link in the Framer-to-Fabric direction, are identical to that provided in Fabric-to-Framer direction, there is only one definition of a TDM-P link. It is applicable for either direction of traffic. Separate receive and transmit link definitions are unnecessary. The TDM-P link has the following general characteristics:

1. A TDM-P link is a point-to-point connection between two TDM system devices.

2. The format of a TDM-P link, the TDM-P frame, is a simplification from Telecordia GR-253-CORE [4], ANSI T1.105 [9] and ITU G.707 [5] SONET/SDH frame (see Section 10). A1/A2 bytes are used for framing, the $X^7 + X^6 + 1$ scrambling polynomial is used to ensure rich transition density and B1 is used for link error monitoring. The rest of the frame is built by simple byte interleaving of the aggregated TFI-5 source signals. No byte

rearrangement according to SONET/SDH standardization is performed to keep the implementation as small as possible.

3. All TDM-P links are frequency locked and all TDM-P frames need to be relatively frame aligned within the deskew window of the TDM system. Methods of aligning client signals to the TDM-P frame include pointer processing and multiplexing/demultiplexing and/or through a mapping process.

There is a wide application space for the use of this interface inside a TDM system. It is usable for chip-to-chip connections on a circuit pack as well as for communication between devices over a backplane. An overview of the applications inside a TDM system is shown in Figure 2.

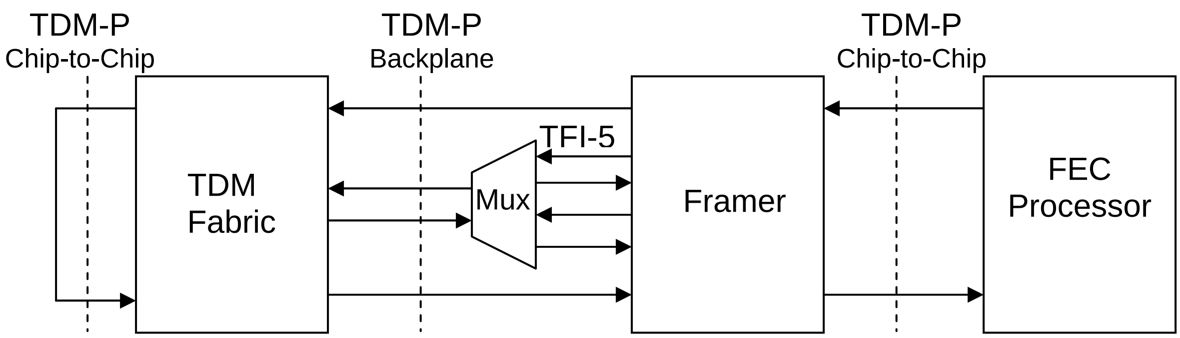

Figure 2: TDM-P Application Overview

7.1 Signal Definition

Similarly to in TFI-5, in TDM-P there are only three signals defined; a data signal (TDMPDATA), a reference clock signal (TDMPREFCK) and an 8kHz frame boundary reference (TDMP8KREF). TDMPREFCK and TDMP8KREF shall be frequency locked to each other with a relative wander of less than +/- 4 UI of TDMPREFCK. TDMPDATA is differential CML, like specified in OIF-CEI [1].

Signal Name	Function
TDMPDATA	The **TDM-P Data** (TDMPDATA) signal carries the data between the Framer and the Switch Fabric. The same signal definition is applicable to data transfer in the Framer to Fabric direction, and the Fabric to Framer direction. Each TDMPDATA link operates at 4.976 Gbps, 6.2208 Gbps or 9.952 Gbps corresponding to the standard SONET STS-96, STS-120 or STS-192 rates and to the standard SDH STM-32, STM-40 or STM-64 rates. Each TDM-PDATA link transports TDM-P frames (the frame format of TFIDATA). Each TDM-P frame is modelled after a SONET / SDH stream. In principle the same mapping format could also be used for higher multiplication factors for rates outside the current scope of OIF-CEI. TDMPDATA is frequency locked to TDMPREFCK.
TDMPREFCK	The **TDM-P Reference Clock** (TDMPREFCK) signal provides timing reference to all the TDM-P data (TDMPDATA) signals in a system. TDMPREFCK is nominally a 155.52 MHz, 50% duty cycle clock. Jitter characteristics of TDMPREFCK do not directly concern interoperability and are beyond the scope of this implementation agreement. All TDMPDATA signals in a system are frequency locked to TDMPREFCK.
TDMP8KREF	The **TDM-P 8kHz Frame Reference** (TDMP8KREF) signal provides reference to frame boundaries for all the devices in a TDM-P system. TDMP8KREF is nominally a 50% duty cycle clock with a nominal frequency of 8kHz. TDMPREFCK and TDMP8KREF shall be frequency locked to each other with a relative wander of less than +/- 4 UI of TDMPREFCK.

Table 1: TDM-P Signal Summary

8 Detailed Description

TDM-P is a SONET/SDH-like system interface, connecting devices electrically according to OIF-CEI [2]. TDM-P uses a frame-based protocol to aggregate 2 or 4 TFI-5 signals into OIF-CEI defined rates.
Figure 3 shows the format of a generic TDM-P frame, where parameter N is the number of STS-1 time-slots (N = 96, 120 or 192).
The orange boxes mark the bytes belonging to the TDM-P link layer. Different to TFI-5, TDM-P does not define a connection layer. The connection layer function can be re-used on TFI-5 source signal basis. The complete white part of the frame is generated by byte interleaving the descrambled TFI-5 source signals. To avoid problems with the transition density of the first SOH row (byte 1 to 2N) the TDM-P scrambler shall leave out only 3 A1 and 3 A2 bytes at position N-2 to N+3 of the TDM-P frame.

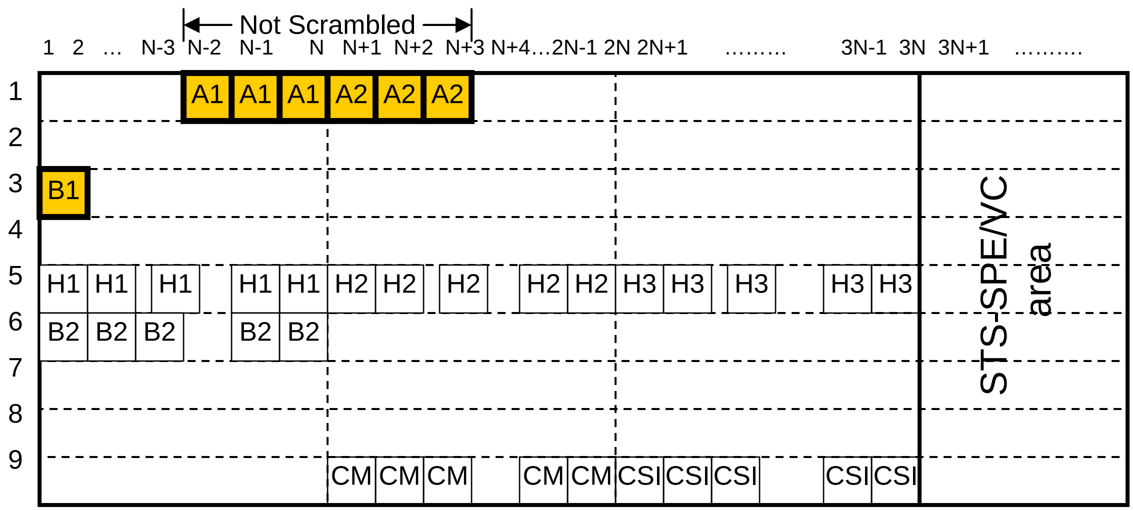

Figure 3: TDM-P Frame Format (Generic)

Figure 4 shows an example, how two TFI-5 client signals @ 2.488 Gbps (STM-16/STS-48 like) will be mapped into the TDM-P frame@ 4.976 Gbps (STM-32/STS-96 like, N=96).
The same scheme will be used to map two TFI-5 clients @ 3.1104 Gbps (STM-20/STS-60) into a TDM-P frame with N=120 (STM-40/STS-120 like), see Figure 5.
Four TFI-5 clients @ 2.488 Gbps will be mapped into a TDM-P frame by multiplexing the four source signals byte-wise in a round robin fashion into an STM-64/STS-192 like frame @ 9.952 Gbps with N=192, see Figure 6.

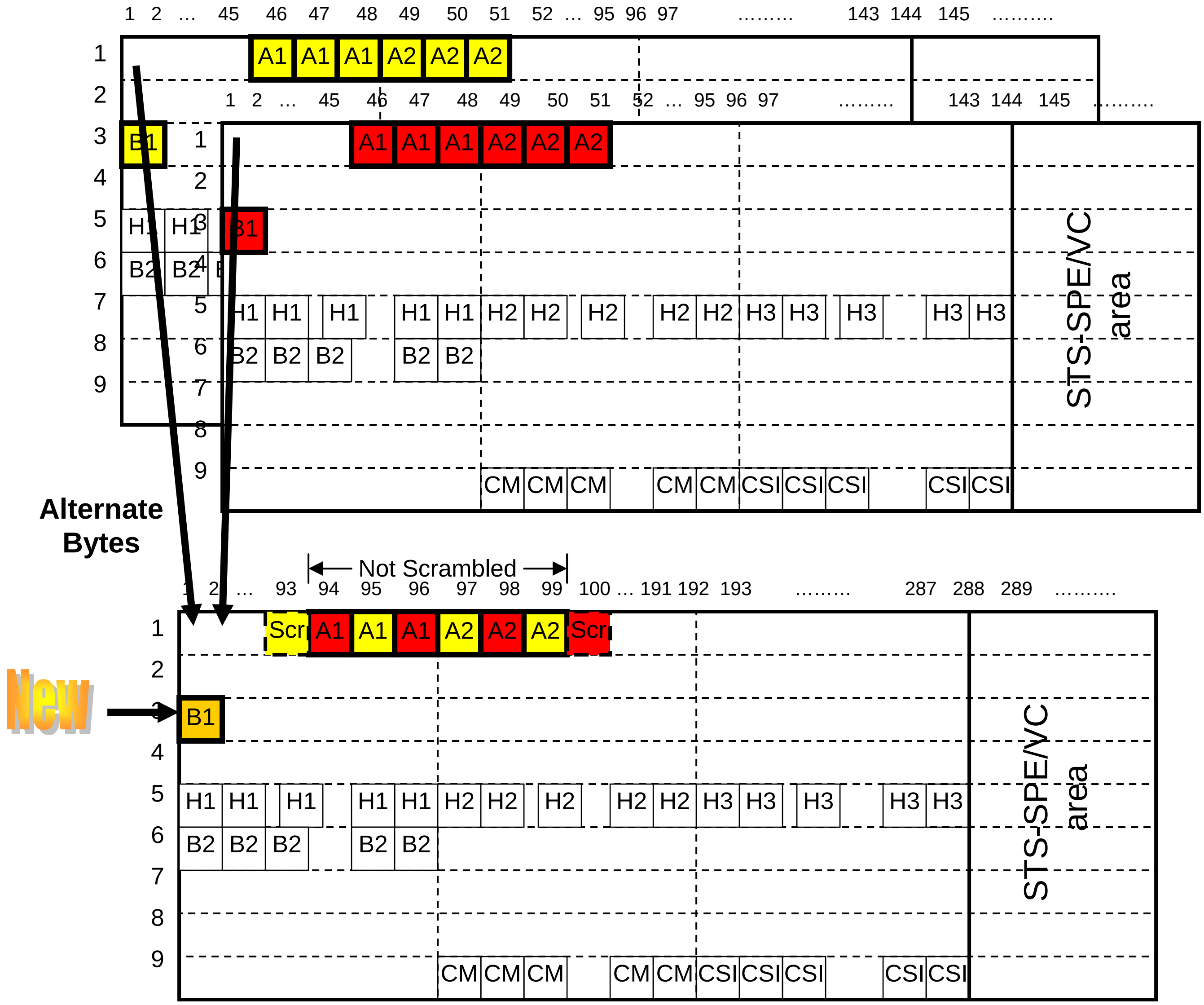

Figure 4: Example: mapping of two TFI-5 clients (STM-16/STS-48 like) into TDM-P frame (STM-32/STS-96 like)

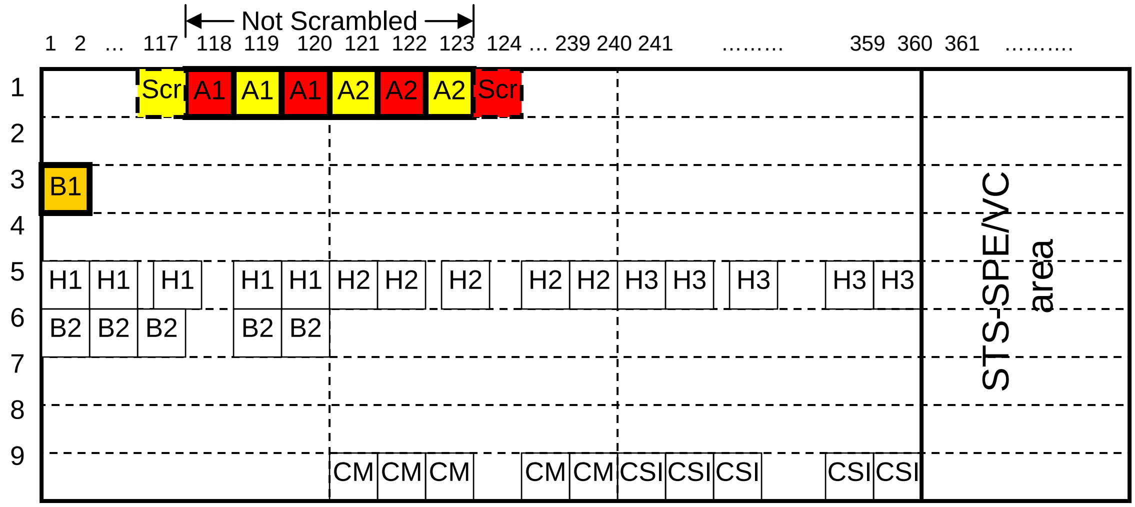

Figure 5: TDM-P frame @ 6.221 Gbps (STM-40/STS-120 like)

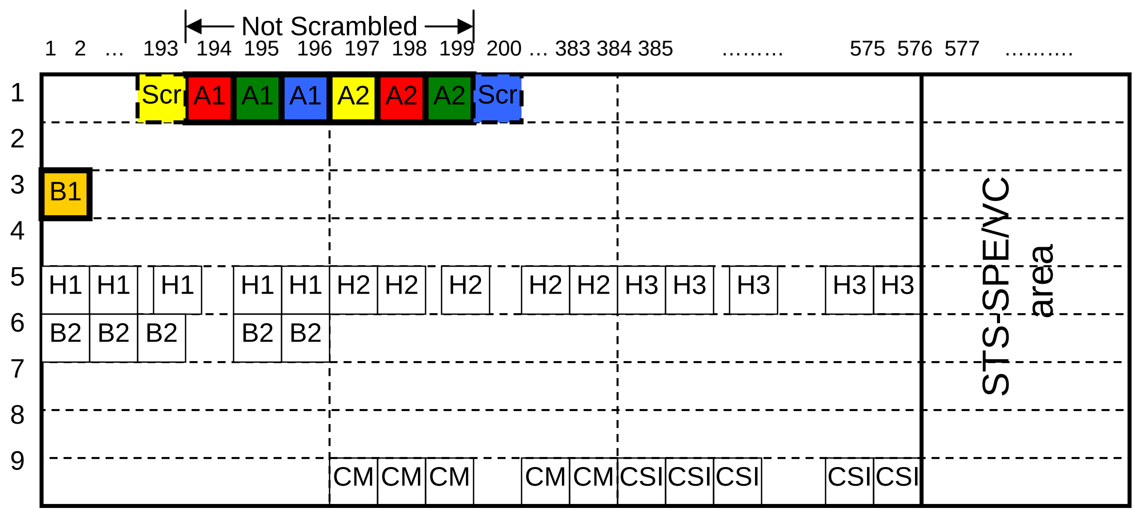

Figure 6: TDM-P frame @ 9.952 Gbps (STM-64/STS-192 like)

8.1 TDM-P Link Layer

The Link layer is generated and terminated at each TDM-P link. The Link layer is independent of the client payload that forms the data stream multiplexed across a group of TDM-P links. The Link layer embodies the electrical signaling and link rate specifications, link framing, link scrambling, link error monitoring and frame deskew functions. The Link layer operates on each link independently.
The Period of transmission of a TDM-P frame is 125 µs. Three different baud rates are defined: 4.976 Gbps (N=96), 6.221 Gbps (N=120) and the standard SONET/SDH 9.952 Gbps (N=192) transmission rate.

The TDM-P 4.976 Gbps frame format is shown in Figure 4; the TDM-P frame format for 6.221 Gbps is shown in Figure 5 and the TDM-P frame format for 9.952 Gbps is shown in Figure 6. The bytes and bits are transmitted as defined in [3], [4], [5]: the order of transmission of the TDM-P frame bytes is first from left to right and then from top to bottom. Within each byte the most significant bit is transmitted first.
The overhead bytes A1, A2 and B1 as shown in Figure 3, Figure 4, Figure 5 and Figure 6 are used by the Link layer for frame delineation and supervision purposes. These bytes are generated by each TDM-P link transmitter (TDM-P link source device) and terminated by each TDM-P link receiver (TDM-P link sink device).

8.1.1 TDM-P Frame Delineation (A1A2 bytes)

The TDM-P frame shall contain three A1/A2 pairs (three A1 bytes followed by three A2 bytes) located in the first row. The three A1 bytes are located in columns N-2, N-1 and N, and the three A2 bytes are located in columns N+1, N+2 and N+3 (N = 96, 120, 192). The source device of a TDM-P link shall insert this 6-byte sequence. The A1 bytes carry the value 0xF6 and the A2 bytes carry the value 0x28.
The sink device of the TDM-P link locates the TDM-P frame boundaries by searching for the framing pattern contained In the A1 and A2 bytes as defined above. Implementations of TDM-P framers may frame on a subset of the 3 A1 and 3 A2 bytes. It is recommended to use at least 2 A1 and 2 A2 bytes.
Upon startup or reset the sink device goes to the OOF (Out Of Frame) state (Figure 7). The sink device shall transition from the OOF state to the INF (In-Frame) state after finding the framing pattern, one TDM-P frame apart (125 µs), for M_1 consecutive frame times. M_1 is defined to be 2 frames in this standard. Once in the INF state, the sink device shall continue to monitor for correct alignment. The sink device of the TDM-P link shall transition from the INF state to the OOF state if the framing pattern is not found (at least one incorrect bit) during M_2 consecutive frames. M_2 is defined to be less than or equal to 5 frames in this standard.

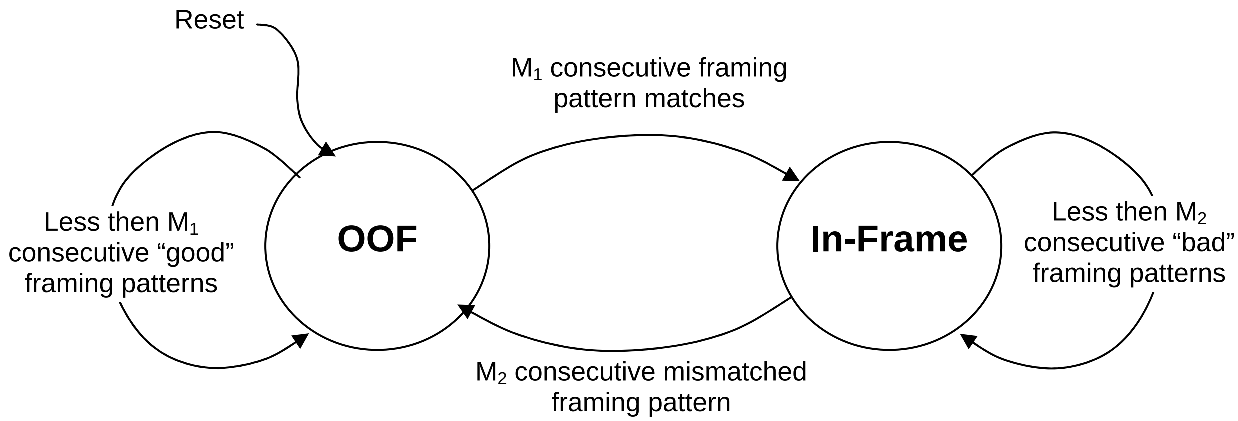

Figure 7: TDM-P State Diagram for Out of Frame and In Frame Conditions

When the sink device of a TDM-P link is in the OOF state, it shall alert the downstream element by overwriting to “all ones” all of the bytes in the Connection and Mapping Layers.

8.1.2 TDM-P Frame Scrambling

TDM-P links are scrambled to ensure rich transition density. The TDM-P link is scrambled with the SONET/SDH polynomial of X7 + X6 + 1. The scrambling is done in a similar way as for a standard SONET/SDH frame, as per [3], [4], [5]:

- The residue of the scrambler is initialized to all ones on the most-significant bit of the byte in row 1 and column [3*N]+1 (N = 96, 120, 192) of the TDM-P frame: this is the first SPE byte of a SONET/SDH frame

In contrast to the SONET/SDH standard the scrambler is enabled in columns 1 to N-3 and N+4 to 3*N (N = 96, 120, 192) of the first row. The bytes in columns N-2 to N+3 (N = 96, 120, 192) are never scrambled, but the scrambler shall continue to run during these byte positions. Columns 1 to N-3 and N+4 to 3*N (N = 96, 120, 192) of the first row of the current TDM-P frame are scrambled with the scrambler running from the reset in the previous TDM-P frame. This “STS-768-like” scrambling mode is used to assure an adequate number of transitions, as the positions in columns 1 to N-3 and N+4 to 3*N of the first row of the TDM-P frame may have been used by the Mapping layer.

8.1.3 TDM-P Link Error Monitoring (B1 byte)

TDM-P links can be monitored using bit-interleaved (BIP-8) parity for transmission errors. The definition of the B1 byte is lifted directly from [3], [4], [5]. The B1 byte is located in the first column of the second row of the TDM-P frame (see Figure 3) and carries a BIP-8 code using even parity. The BIP-8 is calculated over all the bytes in the previous TDM-P frame after scrambling and is placed in the B1 byte of the current frame before scrambling.
In order to allow fault isolation the BIP-8 shall be calculated and inserted in the B1 byte by the source device of every TDM-P link. The sink device of every TDM-P link shall monitor the B1 byte.

8.1.4 TDM-P Link Deskew

All TDM-P links in a system have 4.976 Gbps, 6.221 Gbps or 9.952 Gbps rate and are frequency locked to a common clock reference (TDMPREFCK). In order to be able to properly time-slot exchange different client payloads from multiple TDM-P links across the fabric interfaces, the frame boundaries of the source links shall be closely aligned.
The start of a TDM-P frame has a relative offset from the rising edge of TDMP8KREF of (T) TDMPREFCK cycles. T shall have a range of 1 full TDMP8KREF cycle, and settable in increments of 8 TDMPREFCK cycles or finer. The framer shall output the first A2 byte (byte N+1) of the frame at offset (T) with a

timing accuracy of +/- 8 TDMPREFCK cycles. Programmable offset (T) only applies to framers. The accuracy applies to both TDM-P framers and switch fabrics.

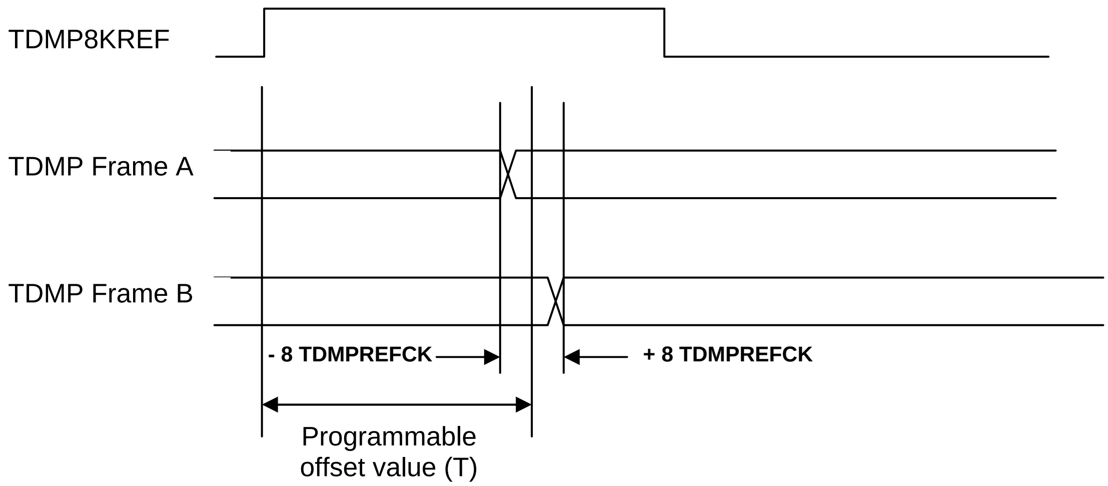

Figure 8: TDM-P frame offset timing

When a set of TDM-P links contains client payloads that are to be switched or multiplexed together, the sink device receiving these links shall be able to tolerate total (skew + relative_wander/2) of at least 128 bytes. The arrival time between the earliest and latest arriving functional links at the sink device shall be less than 128 bytes.
Methods of achieving the standard TFI-5 alignment include pointer processing (retiming), multiplexing/inverse-multiplexing and mapping.

8.2 TDM-P Mapping Layer

The TDM-P Mapping layer provides the transport of the TFI-5 client signals. All the bytes of the TDM-P frame that are not used by the Link layer are available for the Mapping layer (see Table 2).
If bytes of the TDM-P frame are not used by the Mapping or Link layer they shall be undefined except for the bytes 1 to N-3 in row 1, which shall be set to 0xF6 and the byte N+4 to 2*N in row 1, which shall be set to 0x28.

The mapping scheme of the TFI-5 source signals into TDM-P frame is a simple byte multiplexing, e.g. the bytes from two TFI-5 source signals A and B are mapped alternately into the TDM-P frame (A, B, A, B…); the bytes from four TFI-5 source signals A, B, C and D are mapped in a round-robin fashion into the TDM-P frame (A, B, C, D, A, B, C, D…). This mapping scheme is a simplification against SONET/SDH specification, which shall lead to a smaller implementation effort for this protocol.

Type	Name	Positions
Bytes that belong to the Link Layer	A1	Columns N-2 to N of the 1st row
	A2	Columns N+1 to N+3 of the 1st row
	B1	Column 1 of the 2nd row
Bytes that are optionally used by the Mapping layer otherwise they default to 0xF6, 0x28, respectively	-	Columns 1 to N-3 of the 1st row
	-	Columns N=4 to 2*N of the 1st row
Bytes that belong to the Mapping layer for payload transport	All other	

Table 2: Layer Assignments of TDM-P bytes

9 References

9.1 Normative references

[1] Optical Internetworking Forum OIF-TFI-5-01.0, " TDM Fabric to Framer Interface Implementation Agreement", September 16, 2003.

[2] Optical Internetworking Forum OIF-CEI-02.0, " Common Electrical I/O (CEI) – Electrical and Jitter Interoperability agreement for 6G+ bps and 11G+ bps I/O", February 28, 2005.

9.2 Informative references

[3] ANSI - T1.105-1995, "Synchronous Optical Network (SONET) – Basic Description including Multiplex Structure, Rates, and Formats", 1995.

[4] Telecordia, GR-253-CORE, Issue 3 Sept. 2000 – "Synchronous Optical Network (SONET) Transport System: Common Generic Criteria"

[5] ITU, Recommendation G.707 - "Network Node Interface For The Synchronous Digital Hierarchy", 07/09/2000.

[6] ITU, Recommendation G.709 – " Network Node Interface for the Optical Transport Network (OTN)", Feb 2001.

10 Appendix A: Glossary

AISC-P	Alarm Indication Signal Concatenation Indication—Path Layer
AIS-L	Alarm Indication Signal Line Layer
AIS-P	Alarm Indication Signal Path Layer
EXC-MS	Excessive Bit Error—Multiplexed Section Layer
EXC-P	Excessive Bit Error—Path Layer
LOF	Loss of Frame
LOM	Loss of Multi Frame
LOS	Loss of Signal
OOF	Out of Frame
PDI	Path Defect Indication
PLM	Payload Label Mismatch
SD-L	Signal Degrade—Line Layer
SD-P	Signal Degrade—Path Layer
SF-L	Signal Fail—Line Layer
TIM-S	Trace Identifier Mismatch—Section Layer
UNEQ	Unequipped
AC	Alternating current
AIS	Alarm indication signal
AU	Administrative unit
BER	Bit error ratio
C-N	Container of level N
CID	Connection identifier
CM	Connectivity monitoring
DC	Direct current
FDI	Forward defect indication
GE	Gigabit Ethernet
INF	In frame
LAN	Local area network
OC-N	Optical carrier of level N
ODUN	Optical channel data unit of level N
OOF	Out of Frame
OTN	Optical Transport Network
PCB	Printed circuit board
PHY	Physical interface
CSI	Client Status Indication
SDH	Synchronous Digital Hierarchy
SOH	Section overhead
SONET	Synchronous Optical Network
SPE	Synchronous payload envelop
SPI-N	System packet interface of level N
STM-N	Synchronous transport module of level N
STS-N	Synchronous transport signal of level N
TDM	Time division multiplexing
TOH	Transport overhead

VC-N	Virtual container of level N
VCSEL	Vertical cavity
WAN	Wide area network

11 Appendix B: Open Issues / current work items

12 Appendix C: List of companies belonging to OIF when document is approved

ADVA Optical Networking
Aevix Systems
Agere Systems
Agilent Technologies
Alcatel
Altera
AMCC
Analog Devices
Anritsu
Apogee Photonics, Inc.
AT&T
Avici Systems
Azna
Big Bear Networks
Bookham
Booz-Allen & Hamilton
Broadcom
China Telecom
Ciena Corporation
Cisco Systems
CoreOptics
Cortina Systems
Cypress Semiconductor
Data Connection
Department of Defense
Deutsche Telekom
Elisa Communications
Essex Corporation
Finisar Corporation
Flextronics
Force 10 Networks
Foxconn
France Telecom
Freescale Semiconductor
Fujitsu
Furukawa America
Harris Corporation
Hi/fn
Huawei Technologies
IBM Corporation
IDT
Infinera
Intel
JDS Uniphase
KDDI R&D Laboratories
Kodeos Communications
KT Corporation
Lambda Optical Systems
Lattice Semiconductor
LSI Logic
Lucent
Marconi Communications
MCI
MergeOptics GmbH
Mindspeed
MITRE Corporation
Mitsubishi Electric Corporation
Molex
NEC
Nortel Networks
Northrop Grumman
NTT Corporation
Opnext
Optovia
OpVista Inc
PMC Sierra
Quake Technologies
RedC Optical Networks Ltd.
Redfern Integrated Optics, Inc.
Sandia National Laboratories
Santur
SBC
Scintera Networks
Siemens
Silicon Laboratories
Silicon Logic Engineering
StrataLight Communications
Sycamore Networks
Syntune
Tektronix
Telcordia Technologies
Telecom Italia Lab
Tellabs
TeraSea
Texas Instruments
Time Warner Cable
Toshiba Corporation
Tyco Electronics
Verizon
Vitesse Semiconductor
Xilinx

13 Appendix D: Errata

Within OIF TDM-P-01.0 there are mentioned at several occurrences the data rates of TFI-5 and TDM-P data signals. These data rates where rounded to 3-4 digits post cursor and in a few cases a typo was made during this process.
The exact data rates, as mentioned in Section 6, Section 7.1, Section 8, Figure 5, Figure 6, Section 8.1, and Section 8.1.4, shall be compatible with the SONET/SDH defined data rates, namely 2.48832 Gbps, 4.97664 Gbps, 9.95328 Gbps, 3.1104 Gbps and 6.2208 Gbps.