SYNOPSYS®

OIF 448G AI WORKSHOP

448G SerDes, Host and Channel Relationships: Intertwined Opportunities and Challenges

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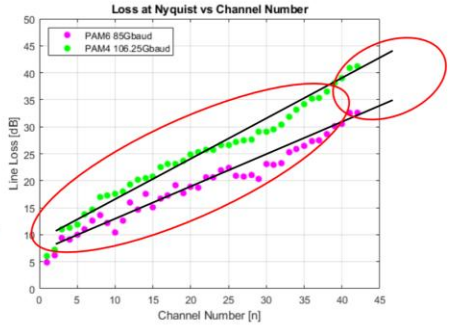
The Road to 448G SerDes

Building on Our Last Discussion

Channel Loss Profile Between PAM4 and PAM6

- Compare loss at PAM4 and PAM6 Nyquist frequency for same physical channel at 224G
- Analyzing at 224G for now, as 448G channels are not available

PAM-4 is better



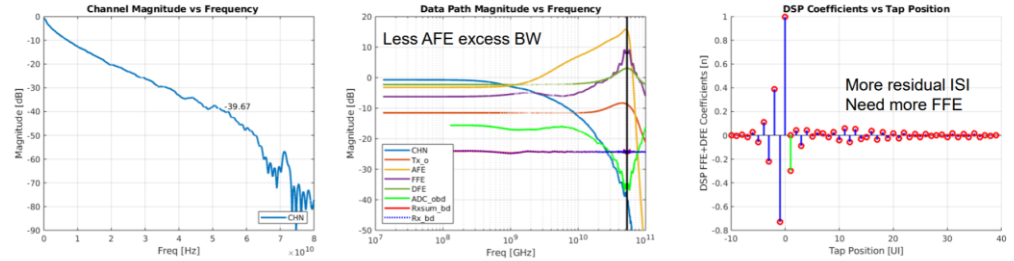
PAM-6 is better
(from equalization perspective, ignores impairments)

- PAM6 has a fixed SNR penalty compared to PAM4
- PAM6 has an increasing advantage over PAM4 as channel length increases.
  - As channel length increases the advantage can outweigh the penalty.
- PHY can do either PAM4 or PAM6 based on industry direction

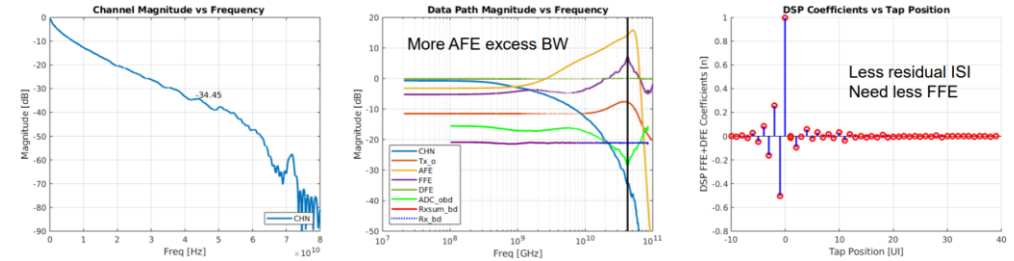
DSP Considerations for 400 Gbps by Kent Lusted et al, Synopsys at SNIA_SFF 400G "AI Workshop" January 2025

Sample Channel and Equalizer Responses

PAM4



PAM6



DSP Considerations for 400 Gbps by Kent Lusted et al, Synopsys at SNIA_SFF 400G "AI Workshop" January 2025

- There are many tools in the toolbox to achieve 448G, and each has advantages and disadvantages
  - Dual-simplex links of PAM4 or PAM6 signaling are the starting point for consideration
- Need host system architecture inputs and channel contributions to support PHY and system studies

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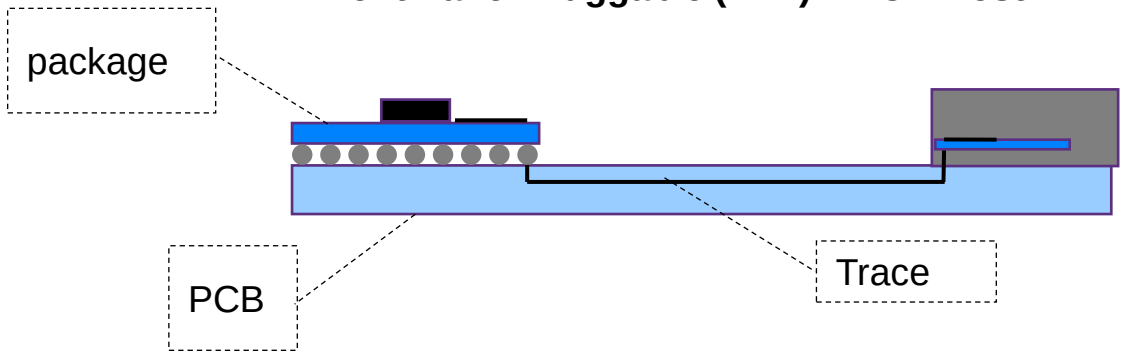
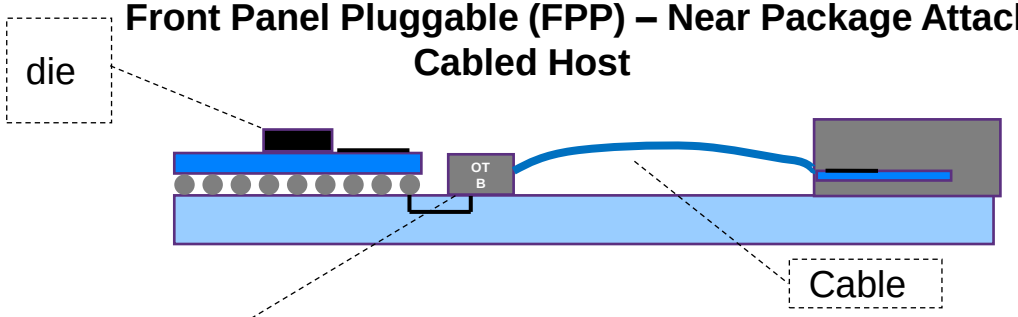
What Will Be The Influence of Host System Architecture at 400 Gbps/lane?

Unretimed Host

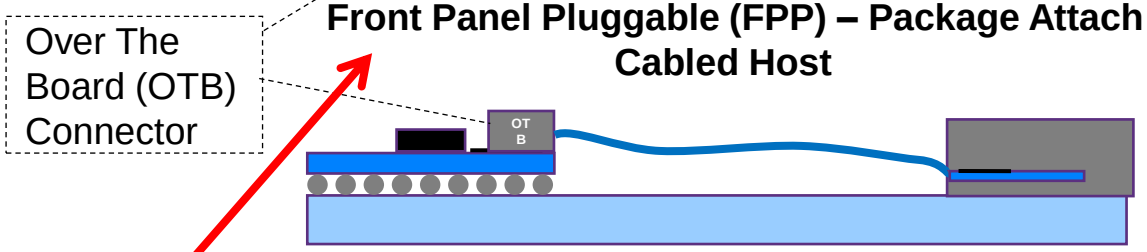
Front Panel Pluggable (FPP) – PCB Host



Front Panel Pluggable (FPP) – Near Package Attach Cabled Host



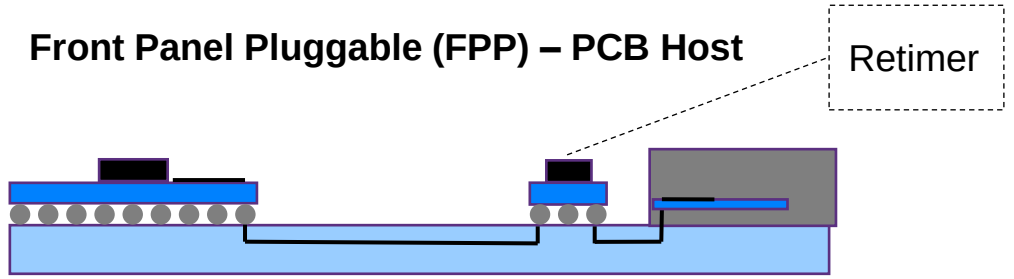
Front Panel Pluggable (FPP) – Package Attach Cabled Host



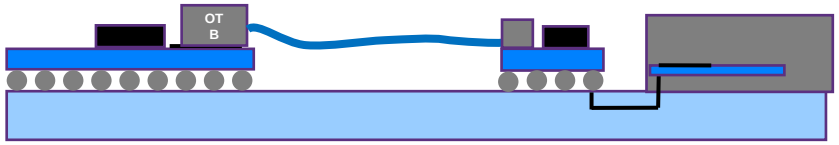
This Work

Retimed Host

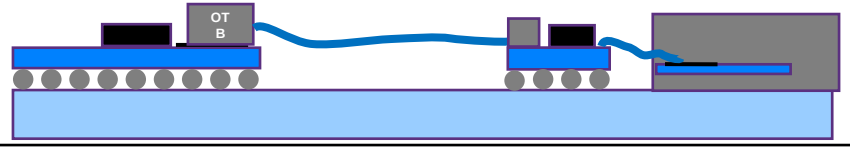
Front Panel Pluggable (FPP) – PCB Host



Front Panel Pluggable (FPP) – Package Attach Cabled Host



Front Panel Pluggable (FPP) – Package Attach Cabled Host



Channel behavior determines the PHY complexity, and vice versa

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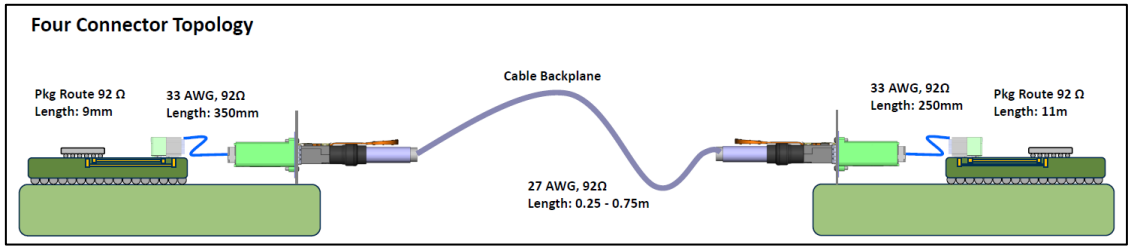
448G Host Channel Topologies Analyzed

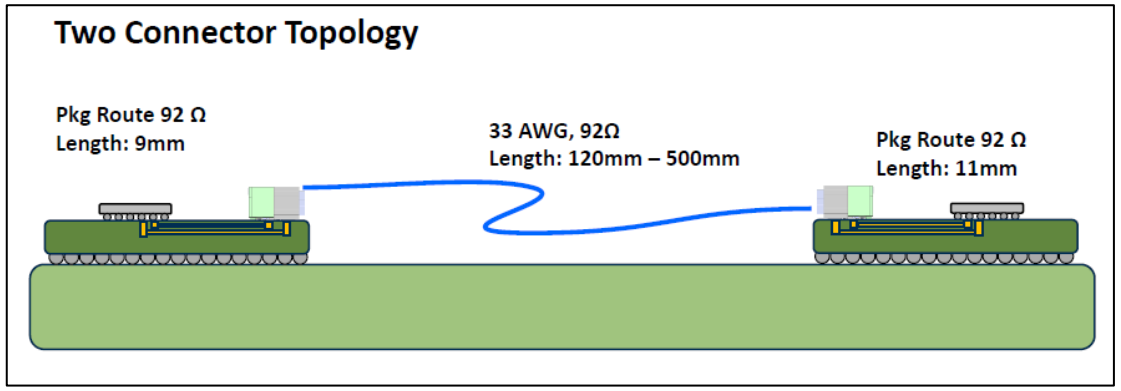
12 Channels Provided by Samtec : 3 Topologies with 4 Lengths Per Configuration

“CableBP”

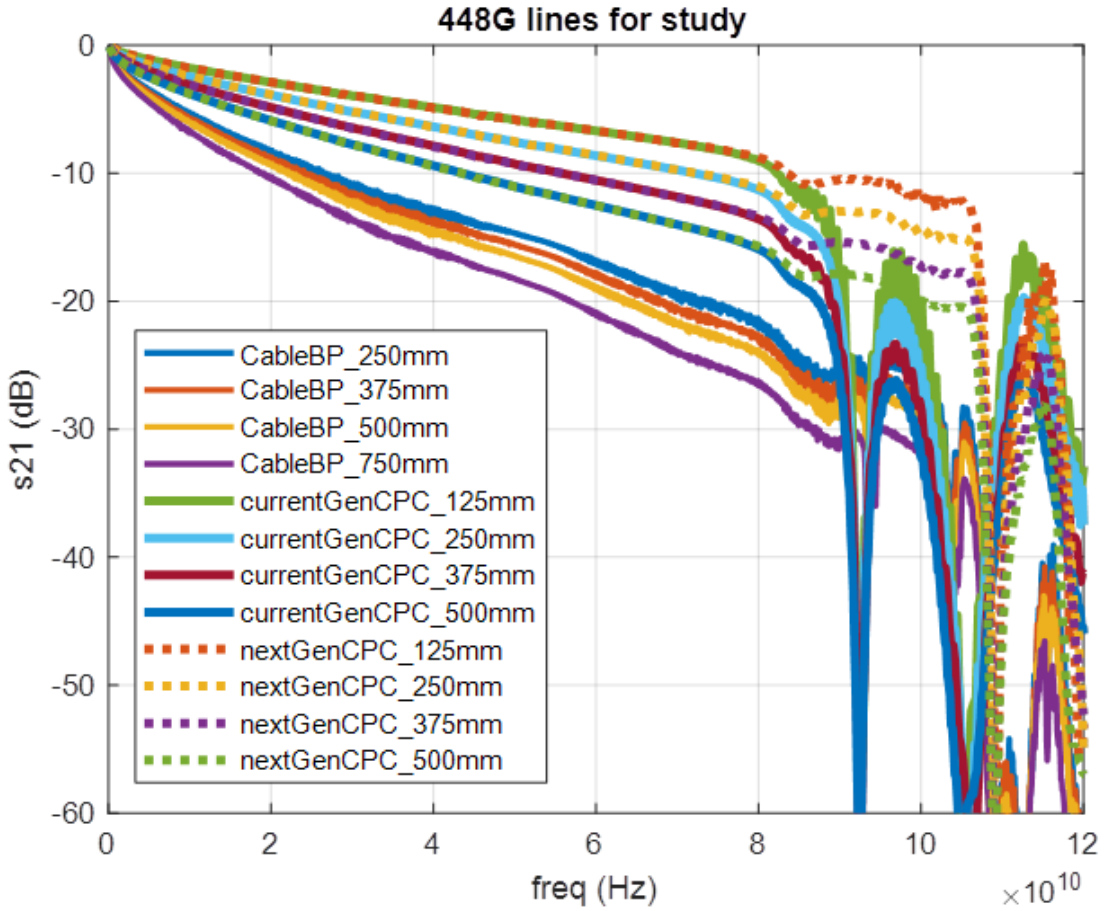


Topology provided courtesy of Samtec

“CurrentGenCPC” “NextGenCPC”



Topology provided courtesy of Samtec



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Statistical Simulation and Analysis of Host System Architecture

- Each channel model was analyzed with statistical eye simulator for 3 configurations
  1. No impairment except for xtalk
     - Make eyes at 1E-6 to show the impact of just the channel
  2. Xtalk from #1 plus adding noise and jitter impairments scaled from 212.5 Gb/s operation
     - Eyes at 1E-4
     - Jitter same on per UI basis
     - Noise spectral density halved since bandwidth doubled
  3. Noise & jitter from #2 **plus** RLM of 0.95
     - Eyes at 1E-4
     - RLM applied to only outer eyes. Worst case is outer eye takes the full brunt.

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Statistical Eye Simulator

- For each Tx eq value (exhaustive sweep)
  - For each timing offset (exhaustive sweep)
    - Adapt CTLE/VGA
    - Adapt DFE and Rx FFE
- Includes all COM impairments
  - Voltage impairments
    - Xtalk pdf created for each xtalker (worst case alignment, 100 pre taps and 2400 post taps)
    - Gaussian pdf for receiver noise (based on eta_0)
    - ADC ENOB (uniform PDF) and full-scale range
    - FFE tap resolution (taps are quantized to give resolution)
  - Jitter Impairments
    - RJ modeled as Gaussian PDF
    - DF modeled as dual dirac
  - No extra package trace, die pad cap or MLSD gain included in today’s results
- Creates eye diagram and reports COM value

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Statistical Simulator Parameter Values for PAM4

Parameter	Setting	Units	Information
f_b	212.5	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d		nF	[TX RX]
L_s		nH	[TX RX]
C_b		nF	[TX RX]
z_p select			[test cases to run]
z_p (TX)		mm	[test cases]
z_p (NEXT)		mm	[test cases]
z_p (FEXT)		mm	[test cases]
z_p (RX)		mm	[test cases]
C_p		nF	[TX RX]
R_0	50	Ohm	
R_d	[50]	Ohm	[TX RX]
A_v	0.4	V	vp/vf=
A_fe	0.4	V	vp/vf=
A_ne	0.6	V	
L	4		
M	128		
filter and Eq			
f_r	0.65	*fb	
c(0)	0.5		min
c(-1)	[-0.1:0.05:0]		[min:step:max]
c(-2)	[0:.025:.05]		[min:step:max]
c(-3)	[0]		[min:step:max]
c(1)	[-0.05:0.05:0]		[min:step:max]
N_b	1	UI	
b_max(1)	0.85		As/dffe1
b_max(2..N_b)	0.15		As/dfe2..N_b
b_min(1)	0		As/dffe1
b_min(2..N_b)	-0.15		As/dfe2..N_b
g_DC	[-13:1:0]	dB	[min:step:max]
f_LF	f_b/40	GHz	
f_z	f_b/2.862	GHz	
f_p1	f_b/1.8839	GHz	
f_p2	f_b	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
Butterworth	.55*f_b	GHz	Rx bw
VGA_max	1.20E+01	dB	ideal vga max value
VGA_step	5.00E-01	dB	ideal vga step size
Rx_FFE_pre	30	taps	pre taps for ffe
Rx_FFE_post	50	taps	post taps for ffe
Rx_FFE resolution	10	bits	tap resolution FFE
timing_sweep	[-.5:.05:.5]	UI	timing sweep
ADC ENOB	8.00E+00	bits	
ADC_fullscale	2.00E+02	mV	peak ADC input

Noise, jitter		UI
sigma_RJ	0.01	UI
A_DD	0.02	V^2/GHz
eta_0	2.05E-09	dB
SNR_TX	33.5	
R_LM	0.95	

CTLE Description
gDC1 =-parms.afe.ctle;
gDC2 = parms.afe.lfeq;
wp1 = parms.afe.wp1;
wp2 = parms.afe.wp2;
wp3 = parms.afe.wLF;
wz1 = parms.afe.wz1*10^(gDC1/20);
wz2 = parms.afe.wLF*10^(gDC2/20);
T = 1/parms.f_b/parms.osr_model;
K = wp1*wp2*wp3/wz1/wz2/(2/T+wp1)/(2/T+wp2)/(2/T+wp3)*10^(gDC1/20)*10^(gDC2/20);
Bctle = conv(conv([wz1+2/T wz1-2/T],[wz2+2/T wz2-2/T]),[1 1])*K;
Actle = conv(conv([1 (wp1-2/T)/(wp1+2/T)],[1 (wp2-2/T)/(wp2+2/T)]),[1 (wp3-2/T)/(wp3+2/T)]);
[Brx,Arx]= butter(4,4/parms.osr_model*.55);
B = conv(Bctle,Brx);
A = conv(Actle,Arx);
filt_pulse = filter(10^(vga/20)*B,A,filt_pulse_in);

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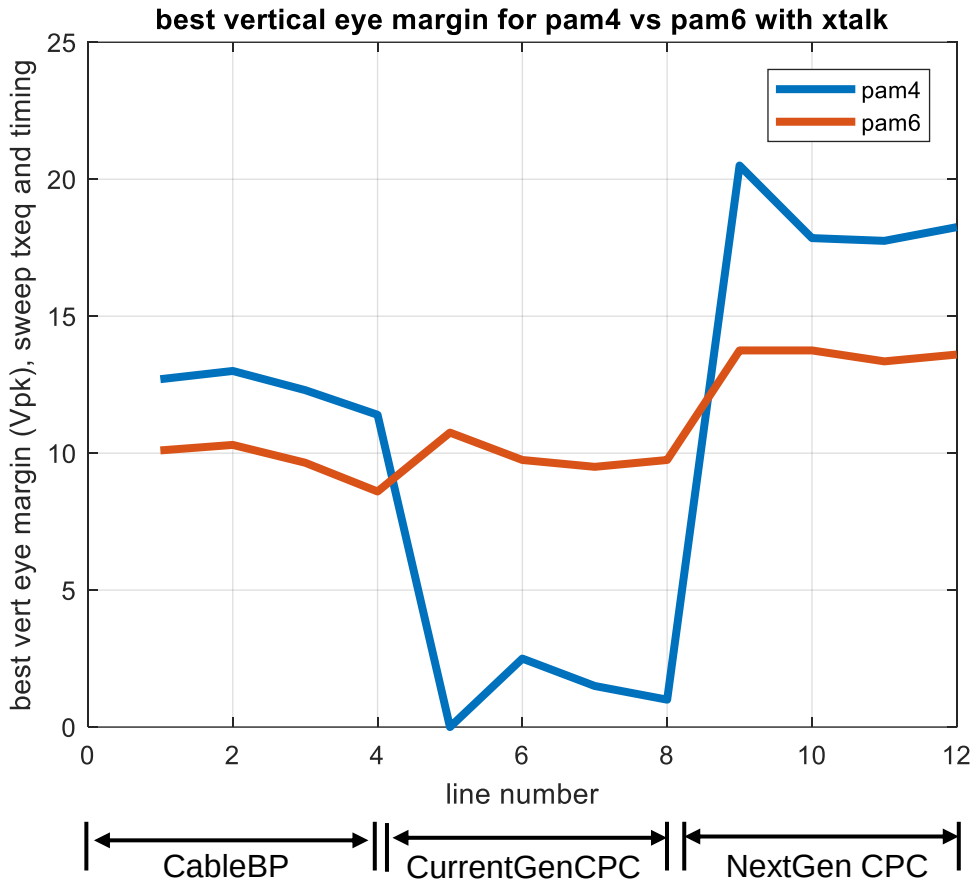
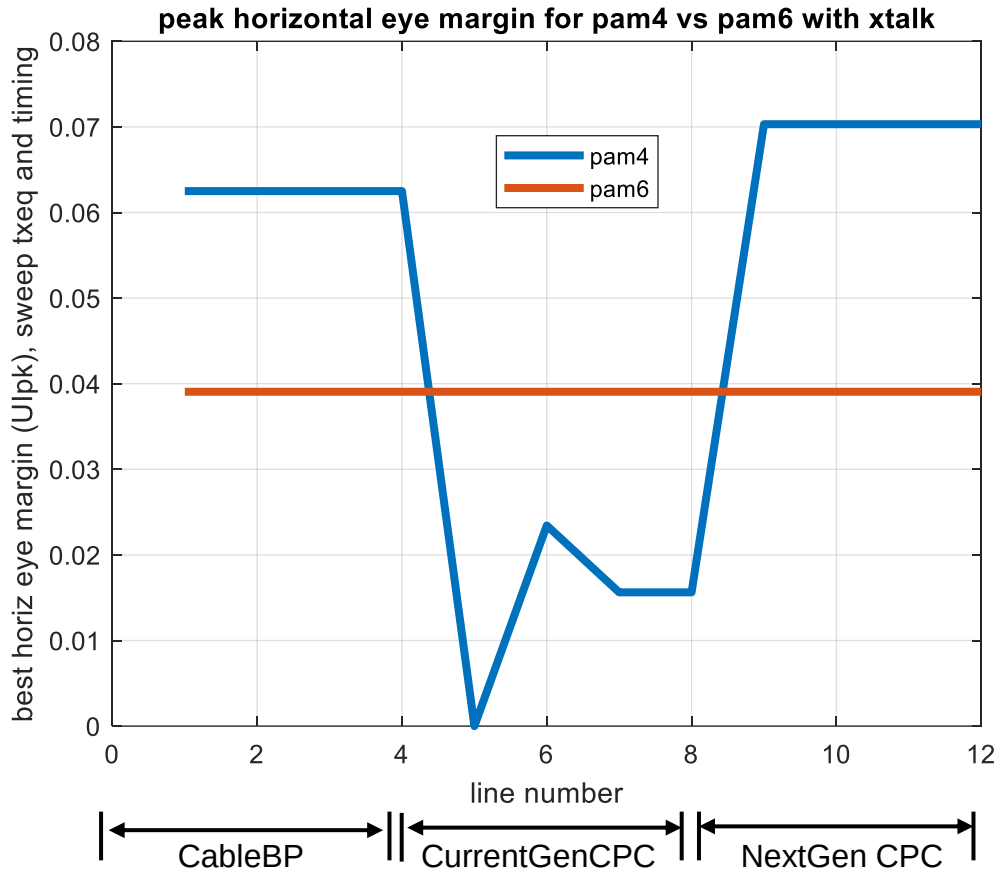
Config #1 : With Only Xtalk

Best Vertical Eye Margin and Horizontal Margin





PAM4 performs better than PAM6 on channels with full bandwidth
PAM6 is better on the band-limited channels (e.g. “CurrentGenCPC”)

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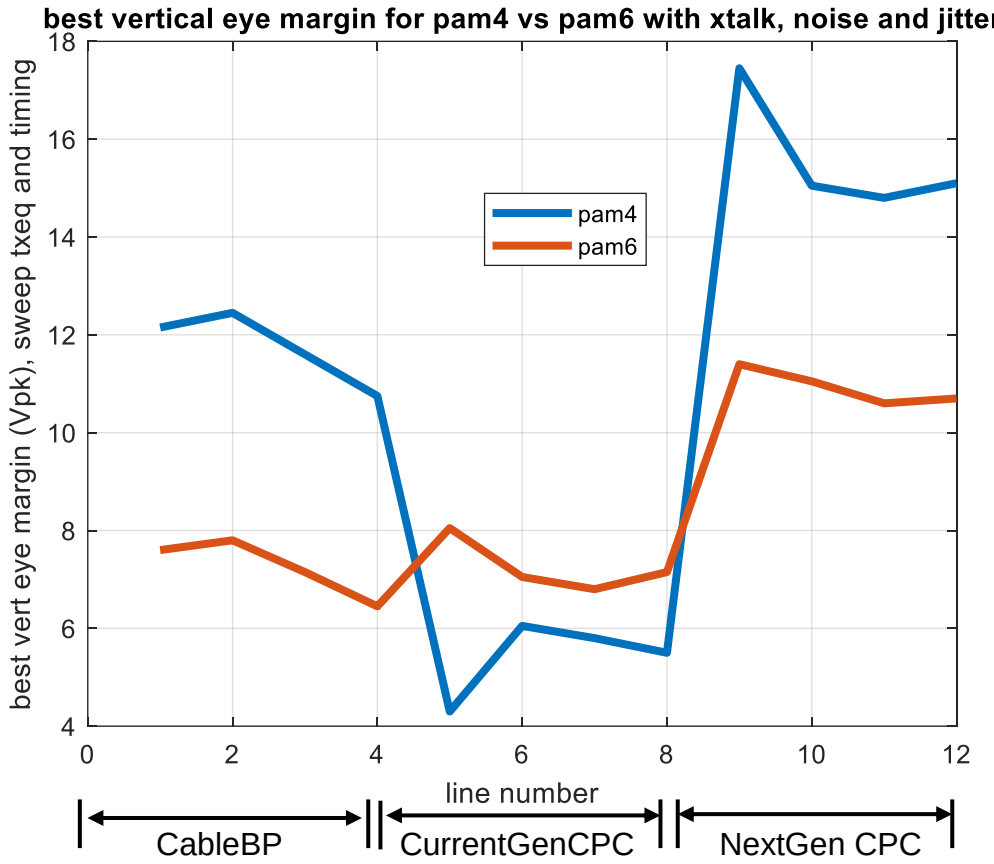
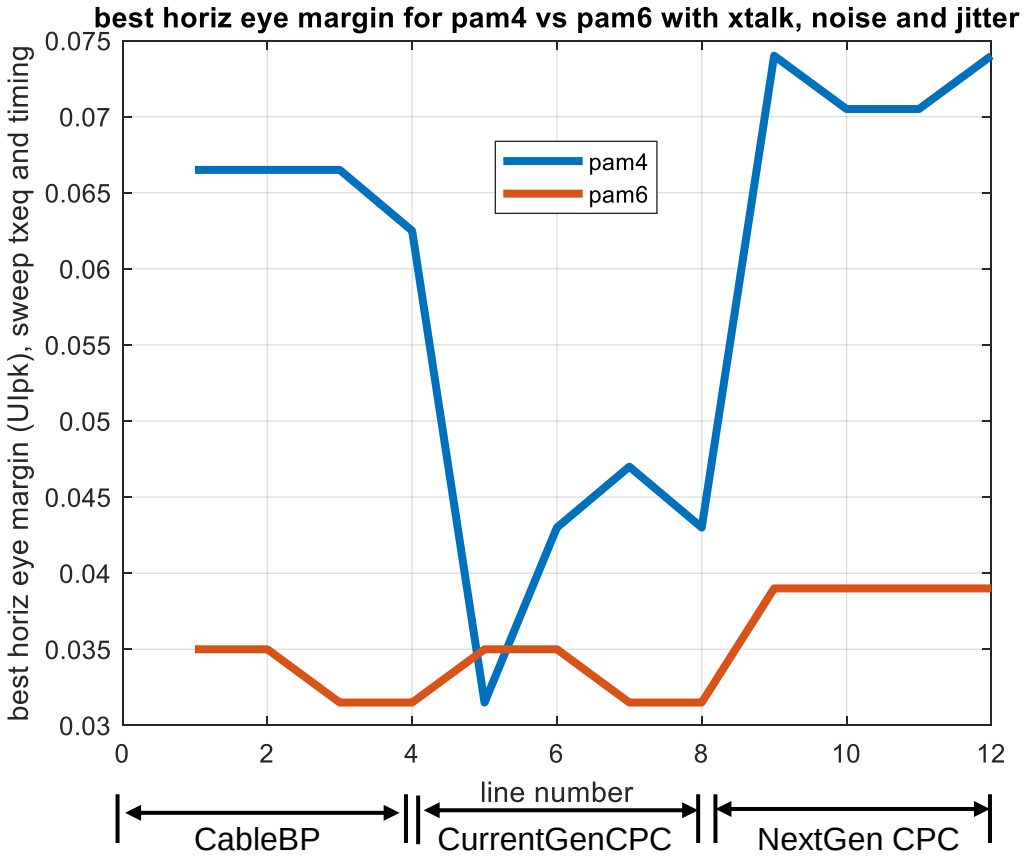
Config #2 : With Xtalk + Jitter + Noise

Best Vertical Eye Margin and Horizontal Margin





Added linear impairments: Note similar relative performance between PAM4 and 6
PAM4 performs better than PAM6 on channels with full bandwidth
PAM6 is better on the band-limited channels (e.g. “CurrentGenCPC”)

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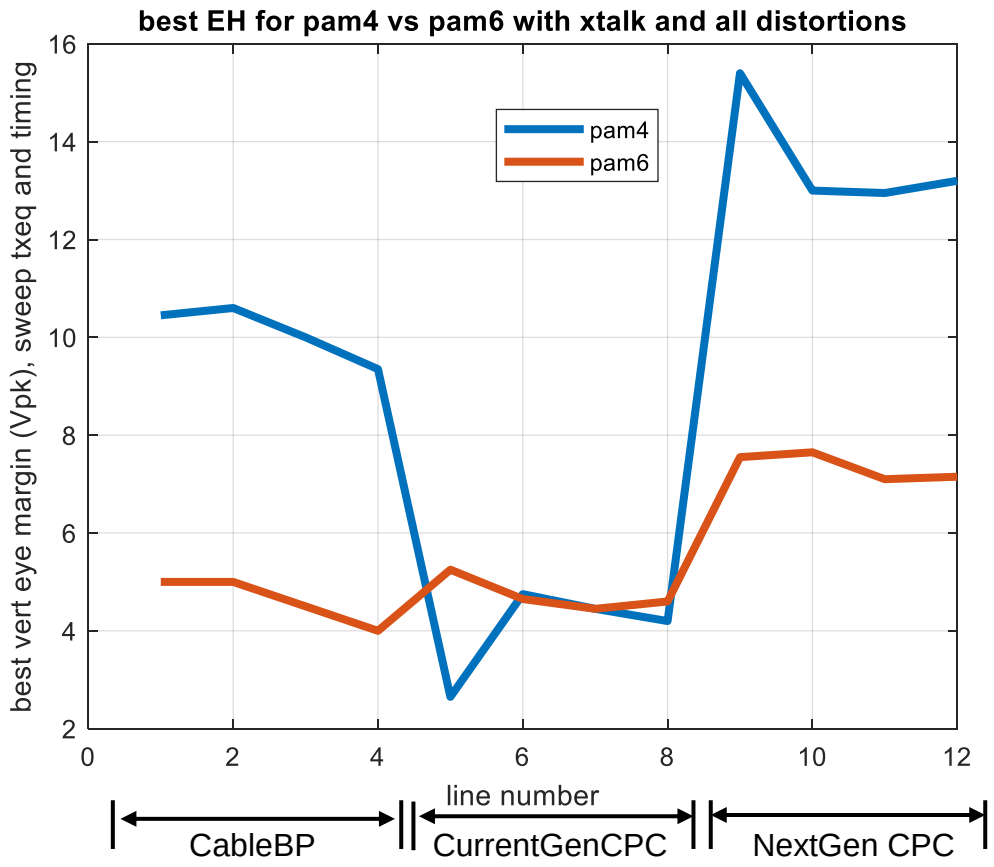
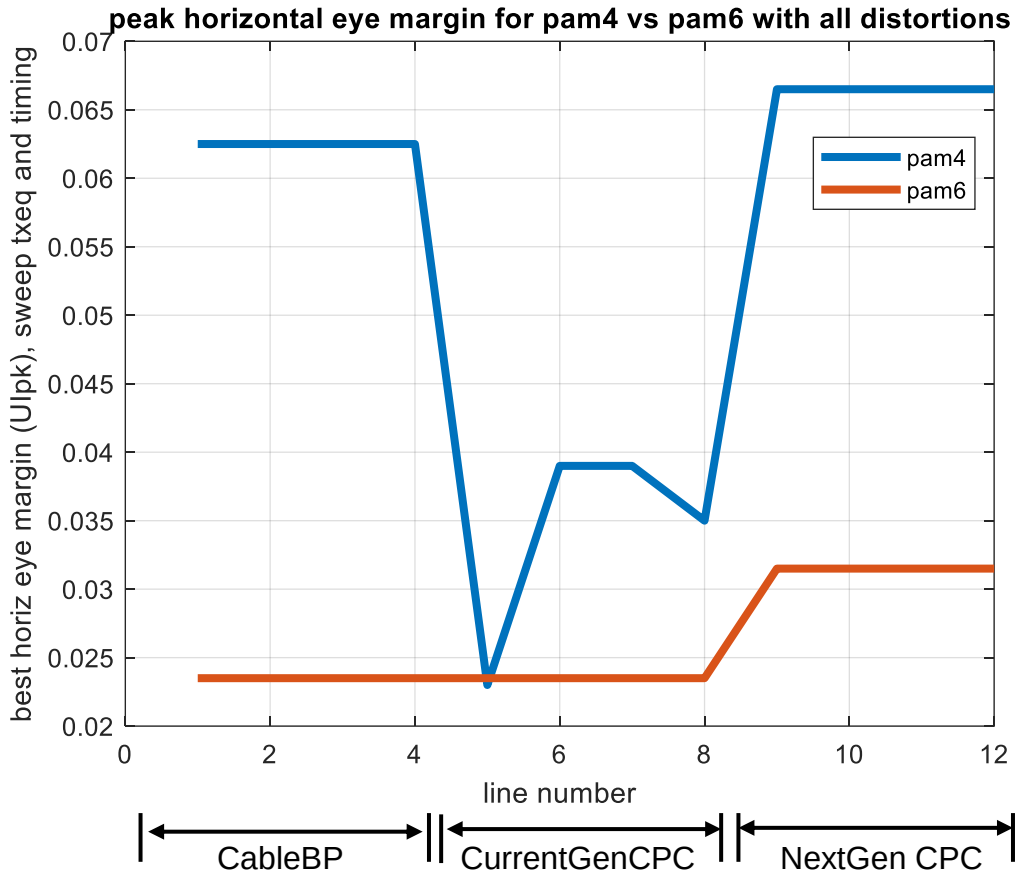
Config #3 : With Xtalk + Jitter + Noise + RLM

Best Vertical Eye Margin and Horizontal Margin





Outer level being compressed by 0.95 hurts the smaller PAM6 outer eye far more than the PAM4 outer eye

PAM6 advantage goes away on band-limited eyes (e.g. “CurrentGenCPC”)

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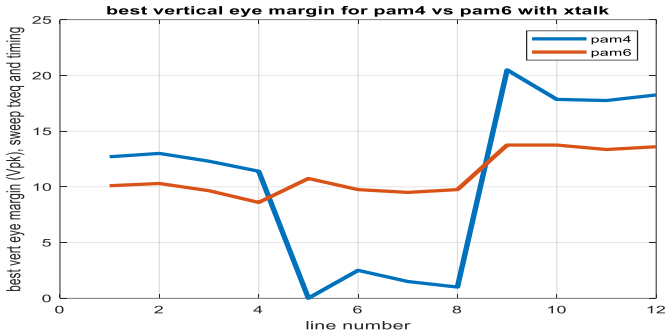
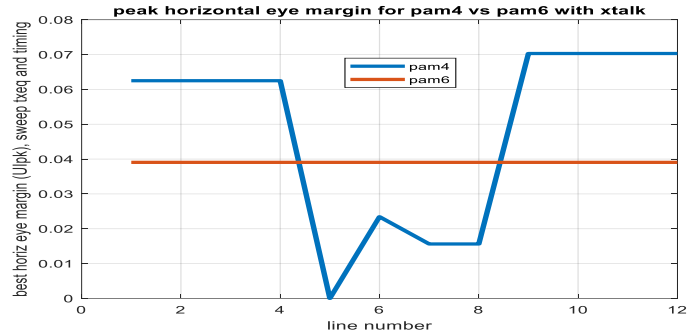
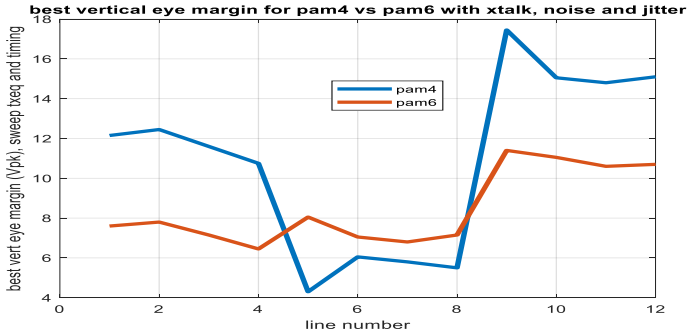
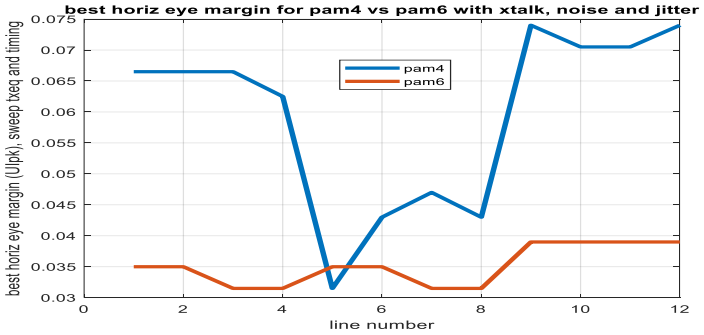
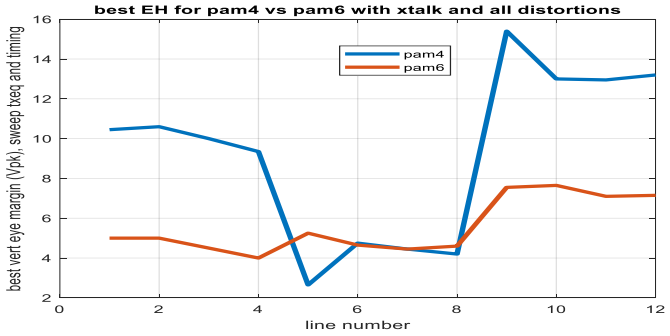
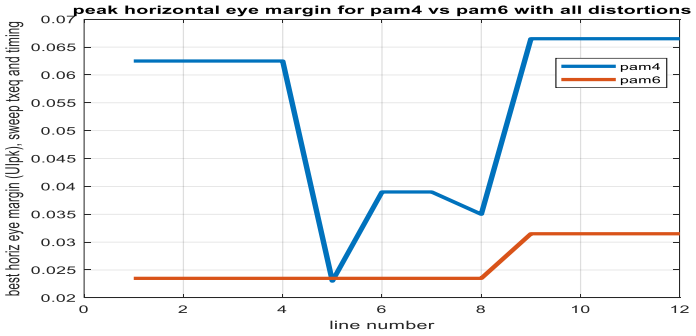
Analysis Summary

Configuration	Vertical Eye Margin PAM 4 vs 6	Horizontal Eye Margin PAM 4 vs 6
Config #1 : With Only Xtalk		
Config #2 : With Xtalk + Jitter + Noise		
Config #3 : With Xtalk + Jitter + Noise + RLM		

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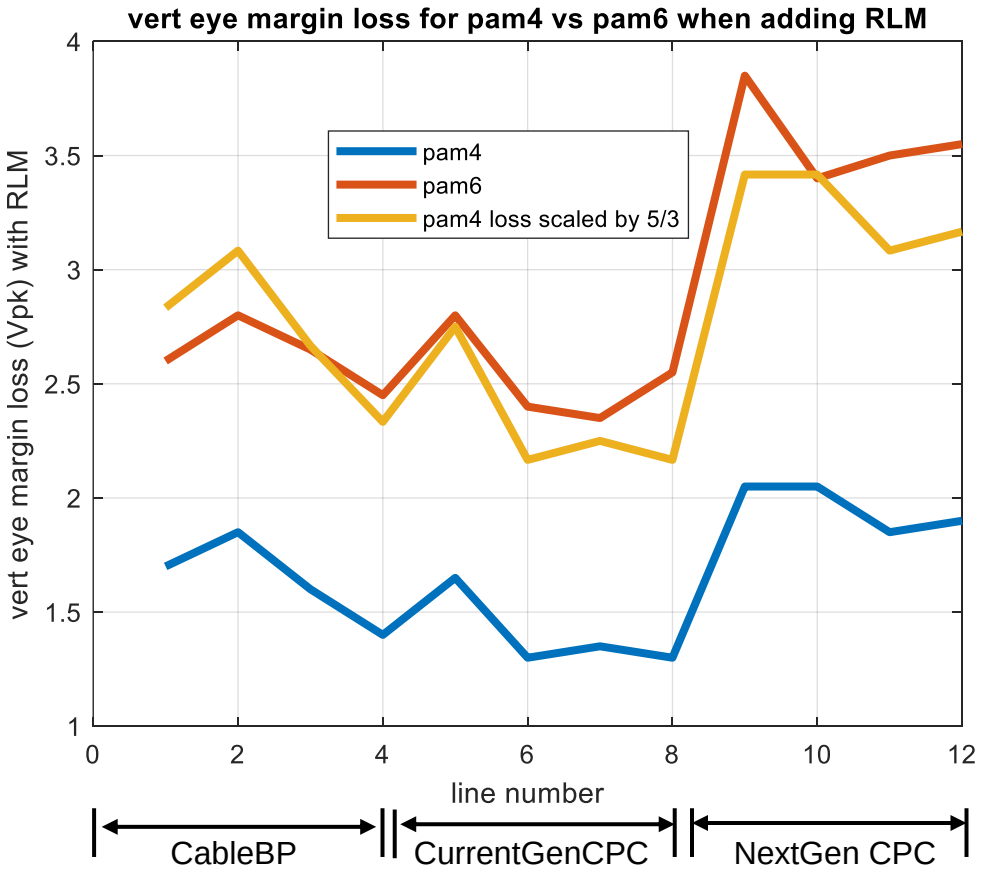
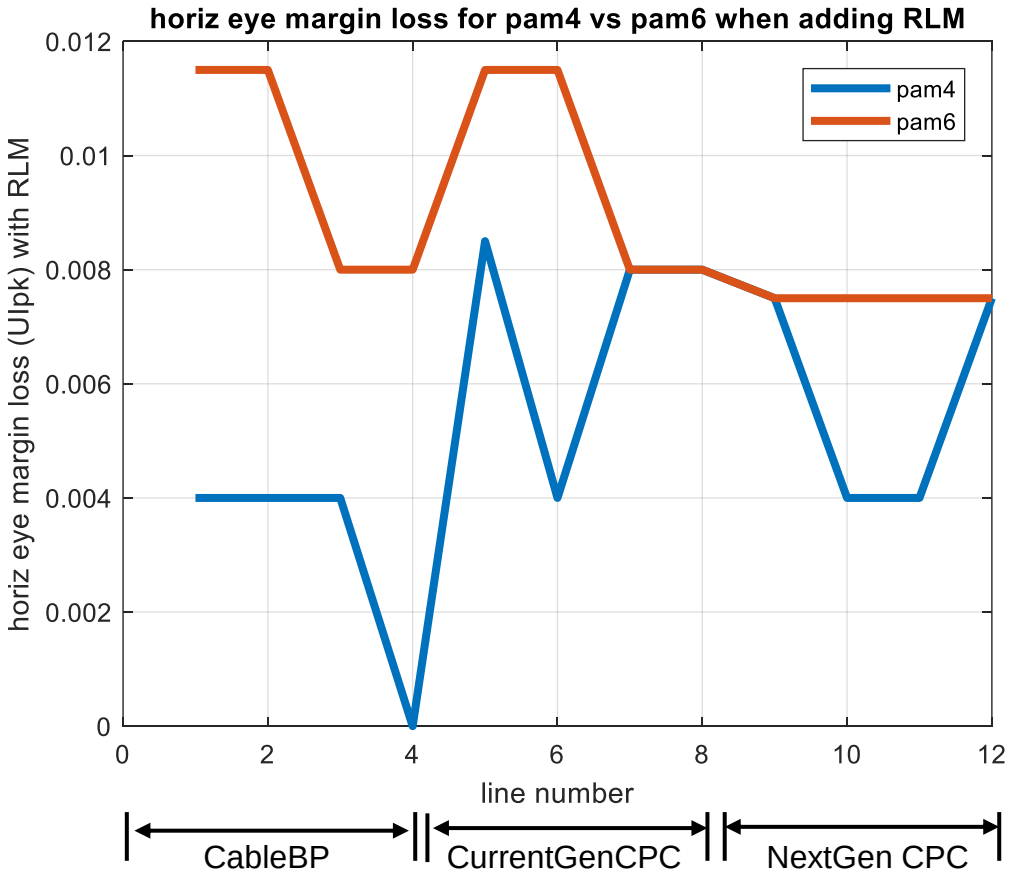
Impact of adding RLM: Eye Margin Loss & Horizontal Margin Loss (UIpk) for Each Line





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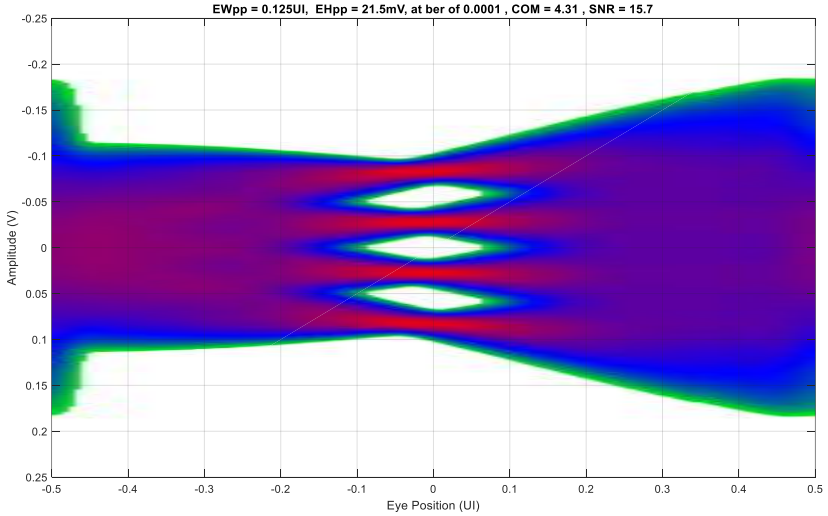
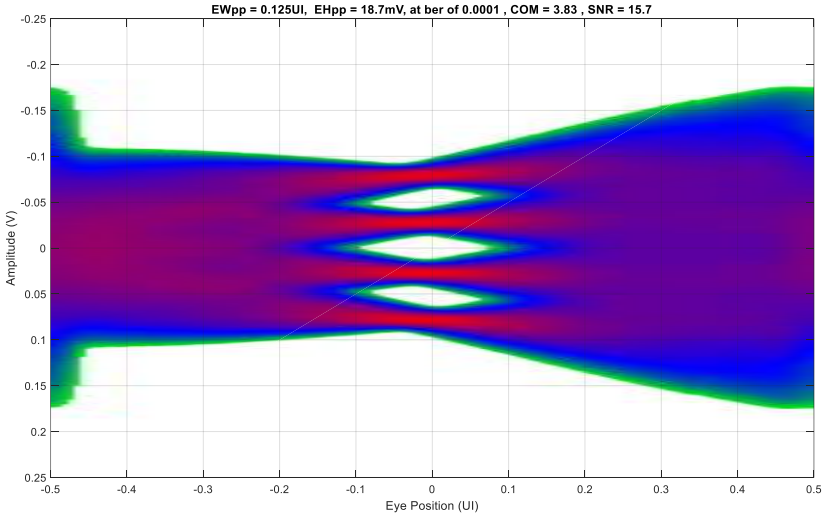
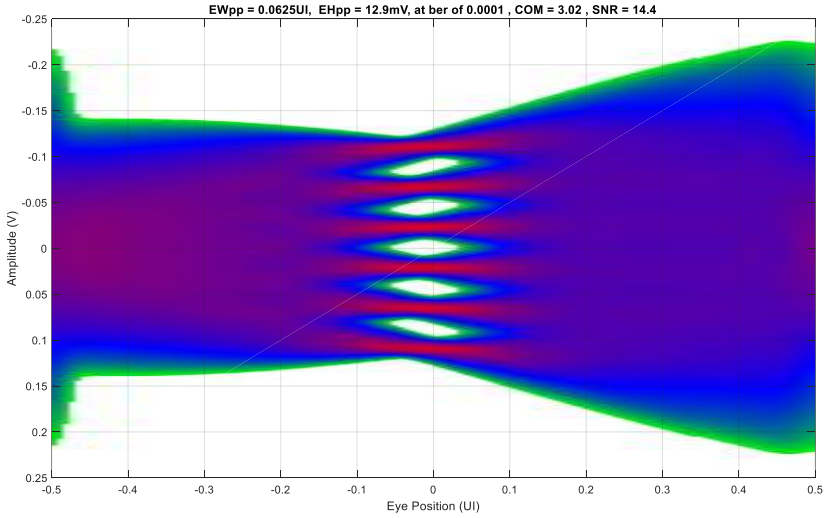
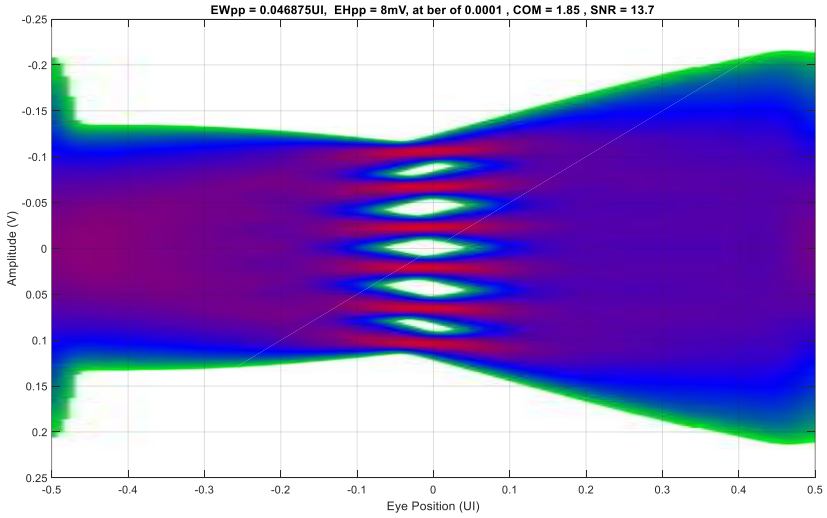
Eye Comparison with and without RLM for CableBP (750mm)

Modulation	Without RLM	With RLM
PAM4		
PAM6		

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Conclusion

- The Host Channel Topology has a significant effect on the results
- Further analysis on PAM4 and PAM6 modulation with added die pad effects and more realistic package traces & breakout is needed
- RLM spec would need to be significantly tightened if PAM6 is adopted
  - To first order an RLM of 0.97 (3/5 of 5%) provides equivalent reduction in performance compared to PAM4
- There are many tools in the toolbox to achieve 448G, and each has advantages and disadvantages
  - Higher circuit element bandwidth with be harder for PAM4. PAM6 will require higher precision in the circuit elements
  - No clear implementation advantage for either approach has been identified to date

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