Preparing for 448G signalling

A test and measurement perspective

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OIF 448Gbps Signaling for AI Workshop
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The path to 448G – a personal view from a test & measurement perspective

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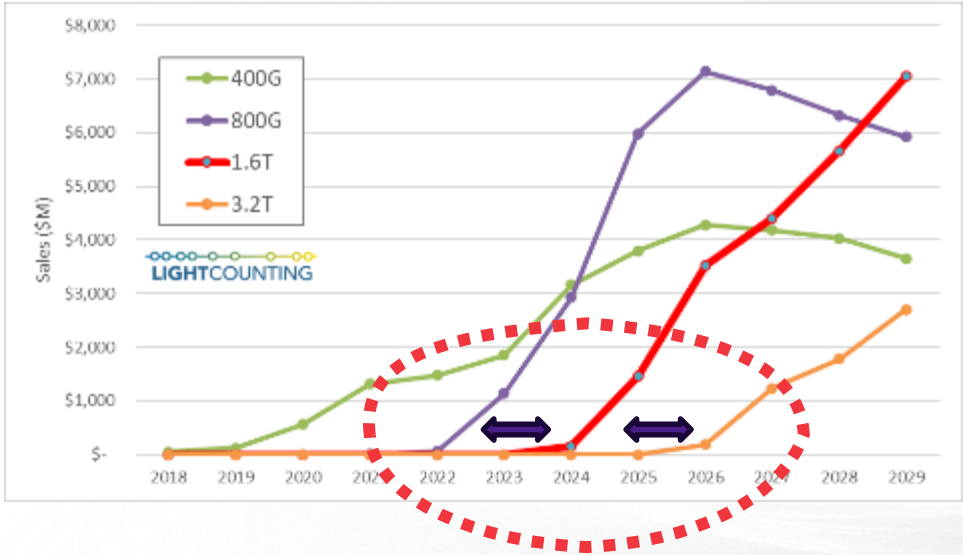
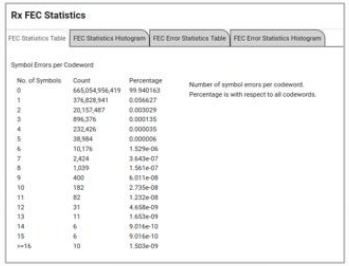
Speed cycles are happening more rapidly

- New speeds coming faster than previous generations!
- Cycles no longer 4-5 years, now ~2 years between speed ramps!
- Time to market in the short R&D and validate stage is critical for success
- Challenging for ROIs and production scaling
- Critical to have good T&M solution – both for rapid development and scale for production



Test and measurement in the product lifecycle



research

R&D

validation

production

deployment

Can it even do that?

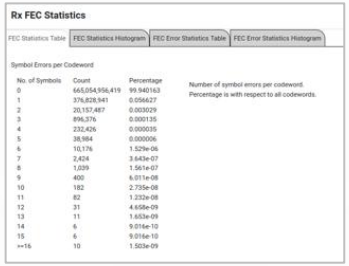
Is it viable?

Can I build it?

Can I manufacture it?

Can I deploy it?

Test and measurement in the product lifecycle



validation

production

R&D

research

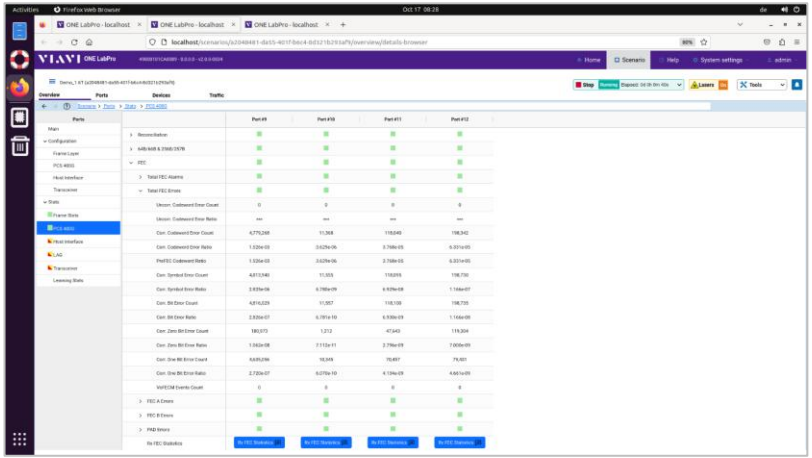
deployment

224G

448G

Today – 1.6Tb & 224G PHY

- Full feature BER and traffic generation shipping since October 2024
- Initial focus has been module and interconnect ecosystem, pre-standards and not always Ethernet
- Switch silicon coming mid 2025 – expect huge Ethernet centric growth
- Significantly more challenging than the 56G => 112G transition
- We still have not really started on the bigger Ethernet 802.3 dj with FECi, ILT and standards based inter-op
  - Also expected to drive new challenges



Can I build it…and what is needed for 448G?

- ICs
  - The first devices we typically ‘see’ are PHY and gearboxes
  - We typically need gearboxes as FPGA SERDES ~1 generation behind PHY speeds
  - Rather not ‘double’ gearbox but may have no choice.
- Connectivity
  - While coax is good for early test – support for native form factor comes quickly
  - Native plugs (OSFP-xxx) perform well
  - Plug and go, integrated I^2C, power, cooling
- Standards or at least clear direction
  - Lane speeds & modulation, PPM and skew ranges, FEC type(s)
- Test and measurement
  - Modules and interconnect come first
  - Support for high scale, high density optics test stand already deployed

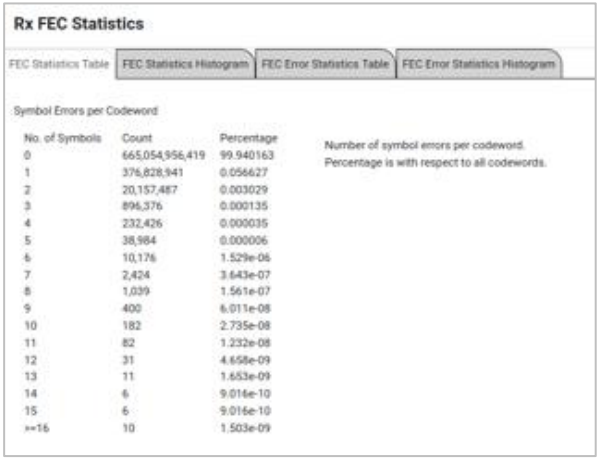
FPGAs remain a major constraint

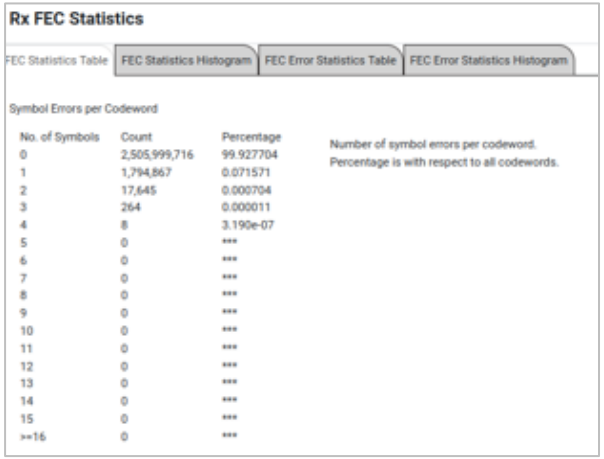
- Today we use the largest possible FPGAs with 112G SERDES for 1.6Tb/224G based T&M
  - A 1.6Tb MAC for T&M applications is huge
    - We need ‘funky’ logic to validate, stress and debug commercial IP and systems
  - 4000 bits wide
  - 8 complete frames in each internal clock cycle
  - Need external gearbox for 224G
- Double gearboxing 112G ⇔224G⇔448G not desired
  - Multiple issues in this approach
- 3.2Tb MAC not viable with current FPGAs
  - But n x 400G/800G/1.6Tb could work

Critical measurements – going beyond BERT

- BER has been the traditional measure of ‘goodness’ for a link
  - Simple set a requirement for a specific BER (in NRZ days – no errors)
- Since PAM-4 we have used FEC
  - But a FEC is not a magic box that turns all 10^-8 into error free
  - Some errors are good, some are bad (AKA – you are making all the right mistakes)
  - We now see significant changes in performance with live traffic for a small change in FEC
- BER + detailed stats vs. framed traffic and FEC tail
  - At 112G and about we find live traffic with live FEC stats best way to tune equalizers
  - But need to dive much deeper than bits
  - 448G we will need error and FEC RX analysis early on

Same BER but very different outcome at 224G





- These actual results taken from a sample OSFP1600 module show two very different live traffic FEC performance BUT they have almost identical unframed PRBSQ31 BER (~10^-8)
- This is a significant factor in setting TX equalization
- Started being an issue at 112G, significant at 224G
- ILT should mitigate

Summary

- Quicker ramps
  - With much greater scale
- Shorter ROI
  - 2 years between new speeds
- PAM-4 and impact of DSP
  - Counting errors (BER) vs deep insight, live traffic
- Need the right components
  - FPGA – fitting a 3.2Tb MAC (or 4 x 800GbE or ….)
  - PHY + Gearbox
- Interconnect remains a major challenge
  - Native plug/form factor
  - Coax and port extension

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