

Preparing for 448G signalling

A test and measurement perspective

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Technology & standards
April 2025

The path to 448G – a personal view from a test & measurement perspective

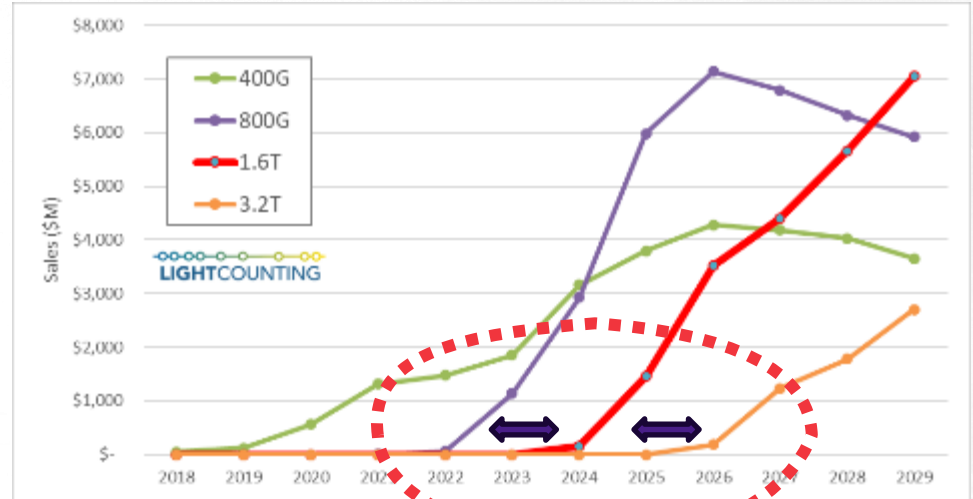
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OIF 448Gbps Signaling for AI Workshop
April 15-16, 2025

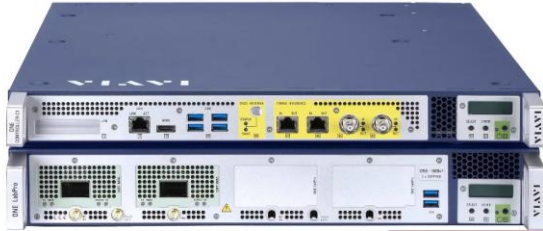


Speed cycles are happening more rapidly

- New speeds coming faster than previous generations!
- Cycles no longer 4-5 years, now ~2 years between speed ramps!
- Time to market in the short R&D and validate stage is critical for success
- Challenging for ROIs and production scaling
- Critical to have good T&M solution – both for rapid development and scale for production



Test and measurement in the product lifecycle



Rx FEC Statistics			
FEC Statistics Table	FEC Statistics Histogram	FEC Error Statistics Table	FEC Error Statistics Histogram
Symbol Errors per Codeword			
No. of Symbols	Count	Percentage	Number of symbol errors per codeword
0	66554956419	99.940163	Percentage is with respect to all codewords.
1	376228461	0.006227	
2	30707487	0.000529	
3	896276	0.000135	
4	232204	0.000036	
5	36584	0.000006	
6	10176	1.529e-06	
7	2428	3.643e-07	
8	1039	1.561e-07	
9	402	6.017e-08	
10	182	2.735e-08	
11	82	1.232e-08	
12	31	4.650e-09	
13	11	1.638e-09	
14	6	9.016e-10	
15	6	9.016e-10	
==16	10	1.503e-09	



research

R&D

validation

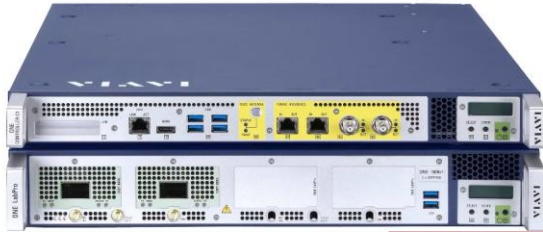
production

deployment

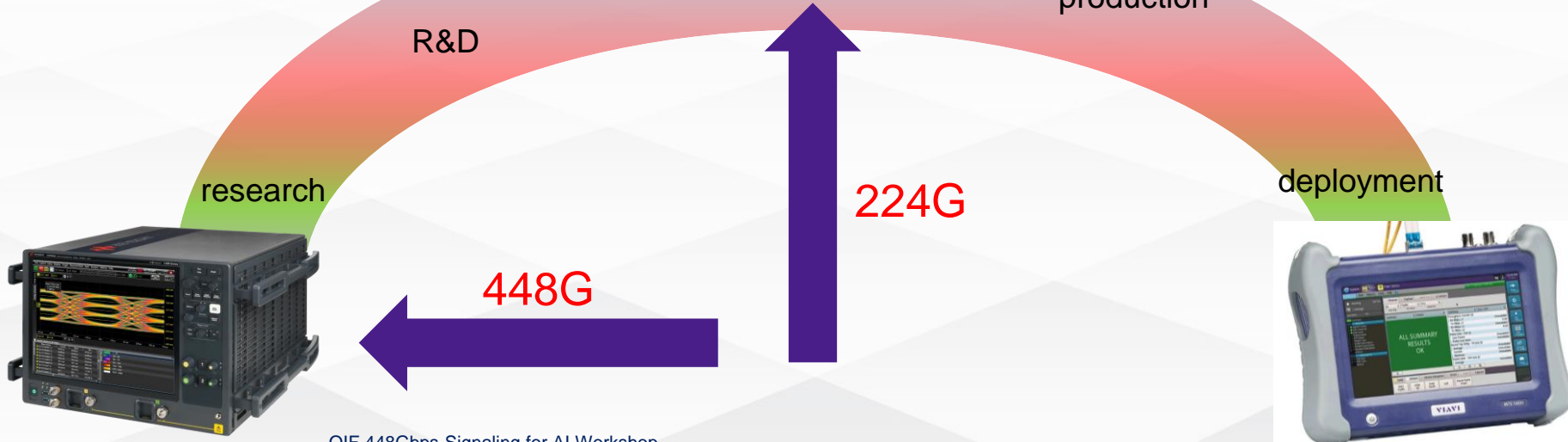
Can it even do that?
Is it viable?
Can I build it?
Can I manufacture it?
Can I deploy it?



Test and measurement in the product lifecycle



Rx FEC Statistics			
FEC Statistics Table		FEC Error Statistics Table	
Symbol Errors per Codeword			
No. of Symbols	Count	Percentage	Number of symbol errors per codeword
0	66554956419	99.940763	Percentage is with respect to all codewords.
1	376328461	0.006227	
2	30197487	0.000209	
3	896376	0.000135	
4	232526	0.000035	
5	36564	0.000006	
6	10176	1.529e-06	
7	2426	3.643e-07	
8	1039	1.561e-07	
9	402	6.017e-08	
10	182	2.735e-08	
11	82	1.232e-08	
12	31	4.650e-09	
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14	6	9.016e-10	
15	6	9.016e-10	
>=16	10	1.503e-09	



Today – 1.6Tb & 224G PHY

- Full feature BER and traffic generation shipping since October 2024
- Initial focus has been module and interconnect ecosystem, pre-standards and not always Ethernet
- Switch silicon coming mid 2025 – expect huge Ethernet centric growth
- Significantly more challenging than the 56G => 112G transition
- We still have not really started on the bigger Ethernet 802.3 dj with FECi, ILT and standards based inter-op
 - Also expected to drive new challenges

Port #1	Port #1B	Port #1I	Port #1O	
Gen. Unicast Error Count	4,775,268	11,388	118,640	198,242
Gen. Multicast Error Rate	1.826e-05	3.627e-06	3.78e-05	6.31e-05
Port1C1 Customized Error Rate	1.826e-05	3.627e-06	3.78e-05	6.31e-05
Gen. Symbol Error Count	4,817,040	91,955	192,219	198,780
Gen. Symbol Error Rate	1.876e-05	3.76e-06	6.49e-05	1.10e-04
Gen. CRC Error Count	4,816,620	10,987	149,110	198,750
Gen. CRC Error Rate	1.876e-05	3.76e-06	6.39e-05	1.10e-04
Gen. CRC Error Count	180,973	1,212	45,843	159,304
Gen. CRC Error Rate	1.868e-08	3.112e-11	3.78e-08	7.06e-08
Gen. CRC Error Count	6,685,054	16,554	76,487	77,401
Gen. CRC Error Rate	2.726e-07	6.076e-10	4.19e-09	4.86e-09
Port1C1 Error Count	0	0	0	0
Port1C1 Error Rate	0	0	0	0
Port1C1 Error Count	0	0	0	0
Port1C1 Error Rate	0	0	0	0



Can I build it...and what is needed for 448G?

- ICs
 - The first devices we typically 'see' are PHY and gearboxes
 - We typically need gearboxes as FPGA SERDES ~1 generation behind PHY speeds
 - Rather not 'double' gearbox but may have no choice.
- Connectivity
 - While coax is good for early test – support for native form factor comes quickly
 - Native plugs (OSFP-xxx) perform well
 - Plug and go, integrated I²C, power, cooling
- Standards or at least clear direction
 - Lane speeds & modulation, PPM and skew ranges, FEC type(s)
- Test and measurement
 - Modules and interconnect come first
 - Support for high scale, high density optics test stand already deployed

FPGAs remain a major constraint

- Today we use the largest possible FPGAs with 112G SERDES for 1.6Tb/224G based T&M
 - A 1.6Tb MAC for T&M applications is huge
 - We need ‘funky’ logic to validate, stress and debug commercial IP and systems
 - 4000 bits wide
 - 8 complete frames in each internal clock cycle
 - Need external gearbox for 224G
- Double gearboxing 112G ⇔ 224G ⇔ 448G not desired
 - Multiple issues in this approach
- 3.2Tb MAC not viable with current FPGAs
 - But n x 400G/800G/1.6Tb could work

Critical measurements – going beyond BERT

- BER has been the traditional measure of ‘goodness’ for a link
 - Simple set a requirement for a specific BER (in NRZ days – no errors)
- Since PAM-4 we have used FEC
 - But a FEC is not a magic box that turns all 10^{-8} into error free
 - Some errors are good, some are bad (AKA – you are making all the right mistakes)
 - We now see significant changes in performance with live traffic for a small change in FEC
- BER + detailed stats vs. framed traffic and FEC tail
 - At 112G and about we find live traffic with live FEC stats best way to tune equalizers
 - But need to dive much deeper than bits
 - 448G we will need error and FEC RX analysis early on

Same BER but very different outcome at 224G

Rx FEC Statistics			
FEC Statistics Table			
FEC Error Statistics Table			
Symbol Errors per Codeword			
No. of Symbols	Count	Percentage	Number of symbol errors per codeword. Percentage is with respect to all codewords.
0	665,054,956,419	99.940163	
1	376,828,941	0.056627	
2	20,157,487	0.003029	
3	896,376	0.000135	
4	232,426	0.000035	
5	38,984	0.000006	
6	10,176	1.529e-06	
7	2,424	3.643e-07	
8	1,039	1.561e-07	
9	400	6.011e-08	
10	182	2.735e-08	
11	82	1.232e-08	
12	31	4.658e-09	
13	11	1.653e-09	
14	6	9.016e-10	
15	6	9.016e-10	
>=16	10	1.503e-09	

Rx FEC Statistics			
FEC Statistics Table			
FEC Error Statistics Table			
Symbol Errors per Codeword			
No. of Symbols	Count	Percentage	Number of symbol errors per codeword. Percentage is with respect to all codewords.
0	2,505,999,716	99.927704	
1	1,794,867	0.071571	
2	17,645	0.000704	
3	264	0.000011	
4	8	3.190e-07	
5	0	***	
6	0	***	
7	0	***	
8	0	***	
9	0	***	
10	0	***	
11	0	***	
12	0	***	
13	0	***	
14	0	***	
15	0	***	
>=16	0	***	

- These actual results taken from a sample OSFP1600 module show two very different live traffic FEC performance BUT they have almost identical unframed PRBSQ31 BER ($\sim 10^{-8}$)
- This is a significant factor in setting TX equalization
- Started being an issue at 112G, significant at 224G
- ILT should mitigate

Summary

- Quicker ramps
 - With much greater scale
- Shorter ROI
 - 2 years between new speeds
- PAM-4 and impact of DSP
 - Counting errors (BER) vs deep insight, live traffic
- Need the right components
 - FPGA – fitting a 3.2Tb MAC (or 4 x 800GbE or)
 - PHY + Gearbox
- Interconnect remains a major challenge
 - Native plug/form factor
 - Coax and port extension



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