448G VSR & LR Channels, Challenges, & Trade-offs

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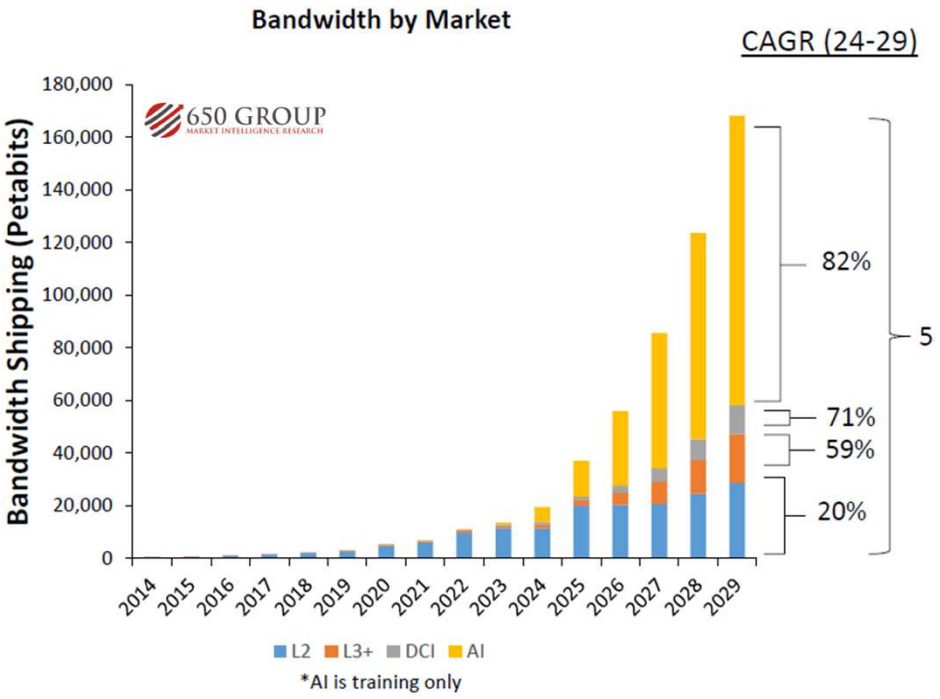
T.E. Connectivity

EVERY CONNECTION COUNTS

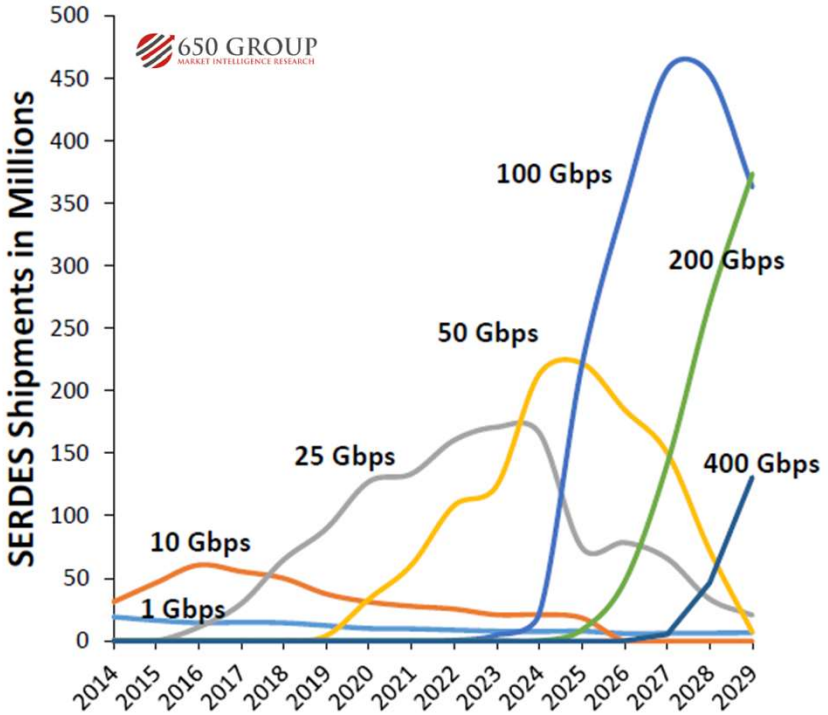
OIF 448Gbps Signaling for AI Workshop
April 15-16, 2025

400G+/Lane Timeline

AI drives growth

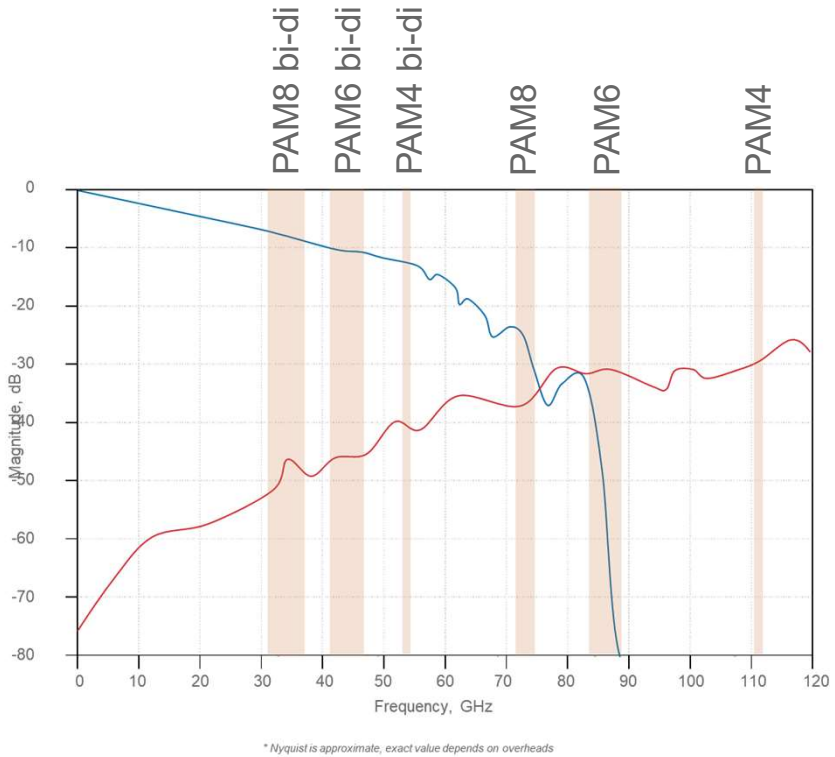


400G+ per lane ramps in 2028



Data courtesy of Alan Weckel, 650 Group

400G+ SI Challenges & Direction



*Frequency response is a typical loss profile, not a specific product.

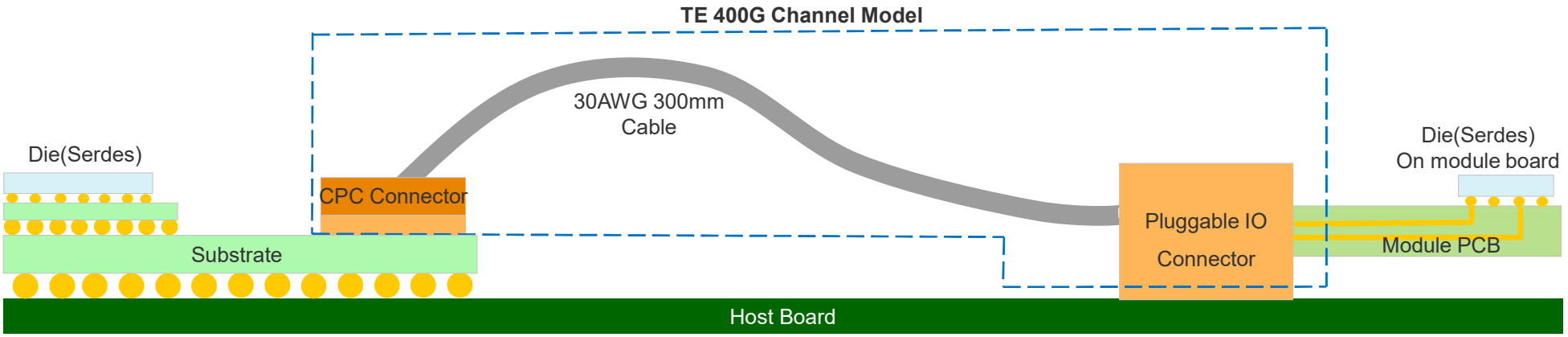
Challenges:

- Reach: Insertion loss limited
  - Bulk cable ~12 dB/m
  - PCB ~2 dB/in
  - Connector ~ 4 dB
- Crosstalk: drive toward -50 dB & below
- Reflections: push ‘suck out’ past Nyquist

Direction: Develop CPC-based optimized channels to minimize impact of loss, reflections & crosstalk for most applications.

Reference: Ashika Pandankeril Shaji, “400Gbps per Channel Pluggable IO Interface Signal Integrity Challenges and Design Considerations,” Ethernet Alliance Technology Exploration Forum, October 22-23, 2024.

VSR Channel



CPC Connector

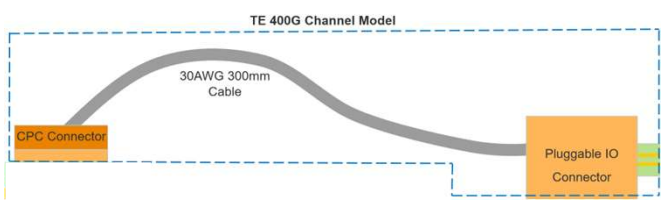
- Includes connection to substrate (device package) and internal cable termination.
- Does not include substrate footprint and breakout.

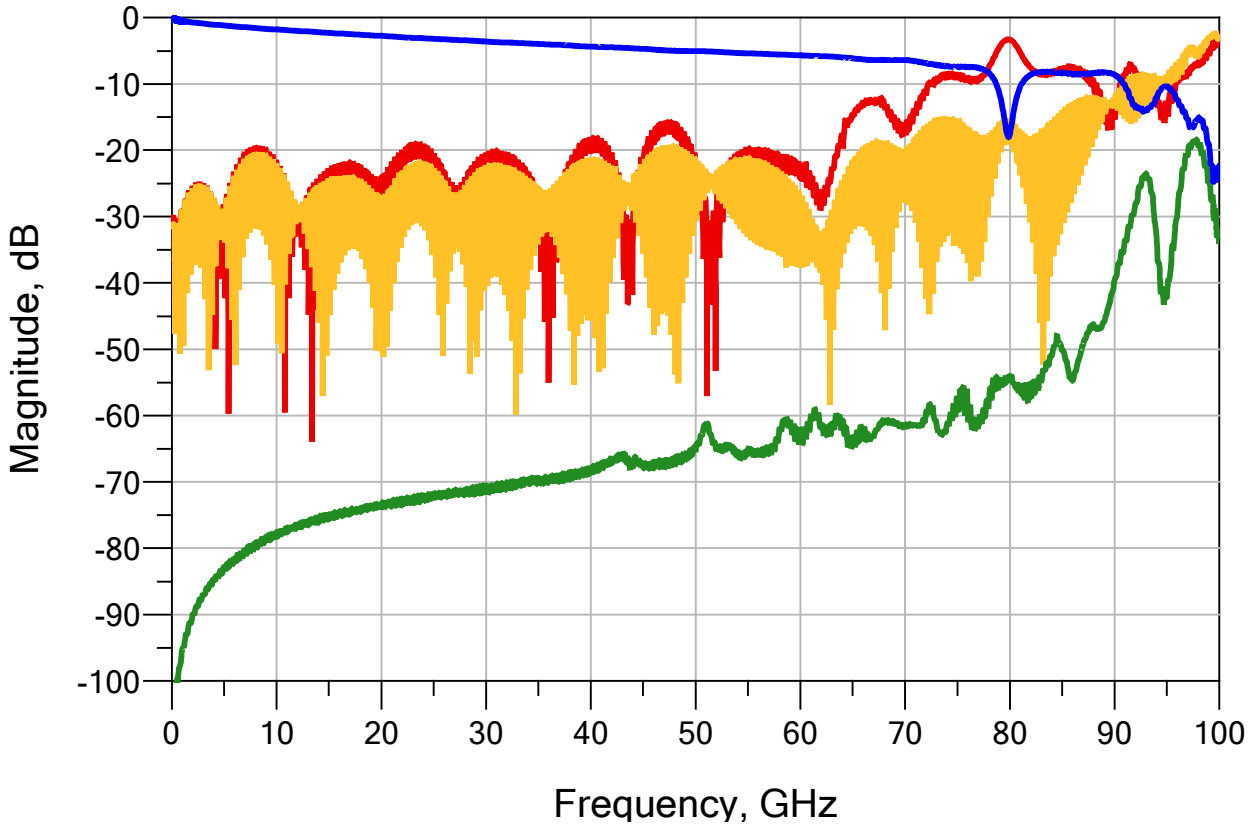
Pluggable IO Connector

- Includes: internal cable termination and short module trace.
- Does not include full trace routing on module board.

Models are preliminary and under development.

VSR Channel



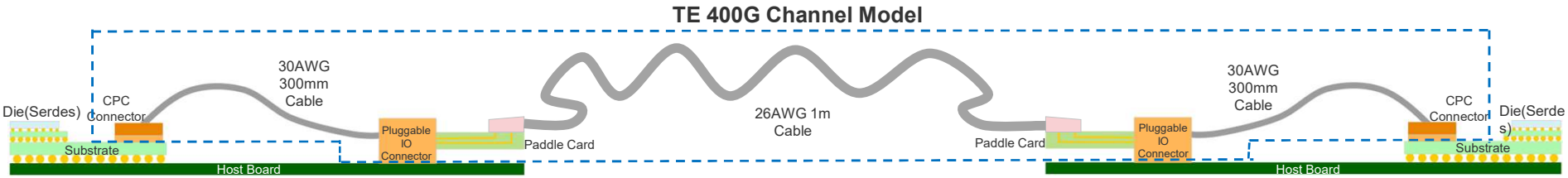


Insertion Loss
Return Loss, Module side
Return Loss, Host side
PowerSum Crosstalk

Crosstalk includes 5 FEXT and 3 NEXT aggressors, module side.

Models are preliminary and under development.

Direct Attach Copper Cable-Based “LR Channel”



CPC Connector

- Includes connection to substrate and internal cable termination.
- Does not include substrate footprint and breakout.

Pluggable IO Connector

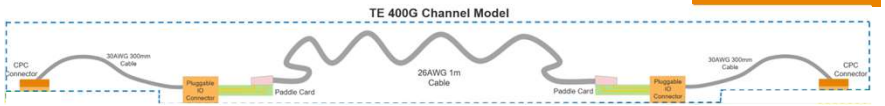
- Includes internal cable termination.

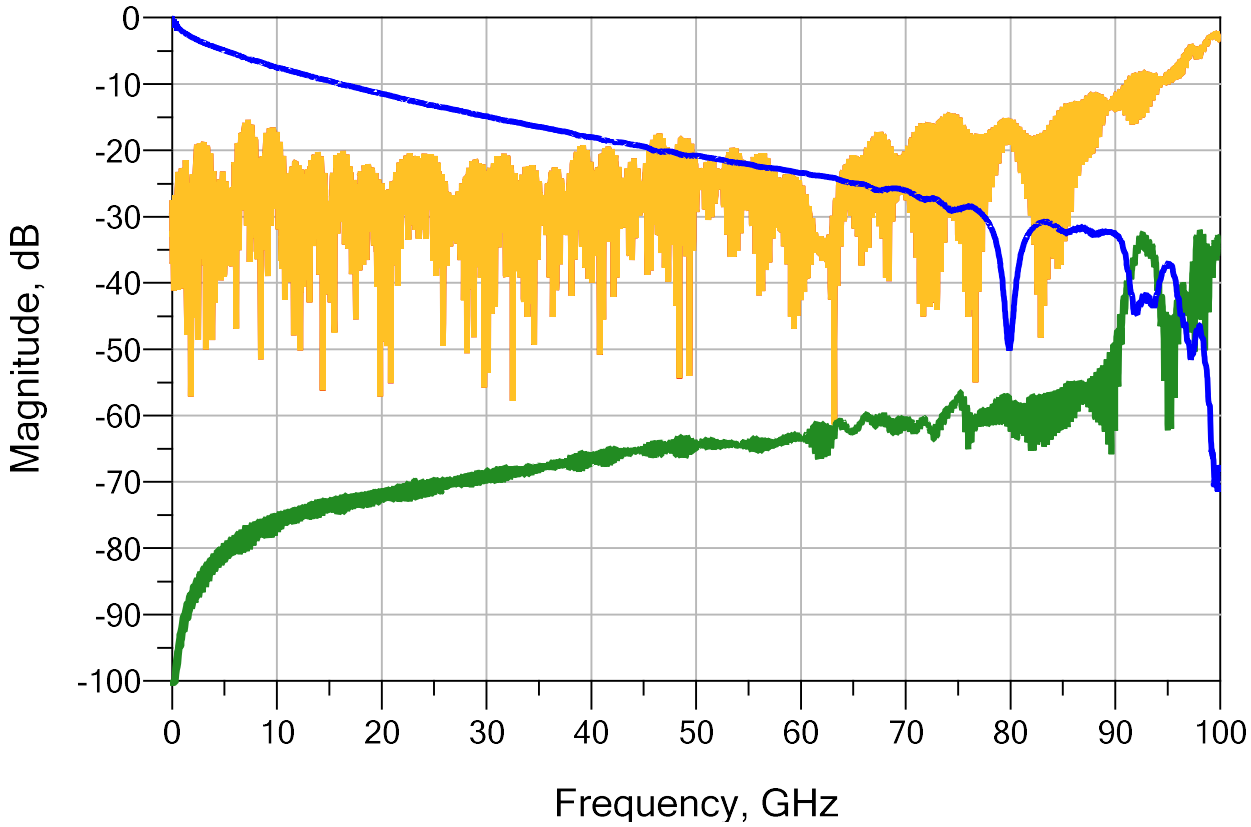
External Cable Assembly

- Includes pluggable module PCB trace, external cable termination & bulk cable.

Models are preliminary and under development.

DACCable-Based “LR Channel”





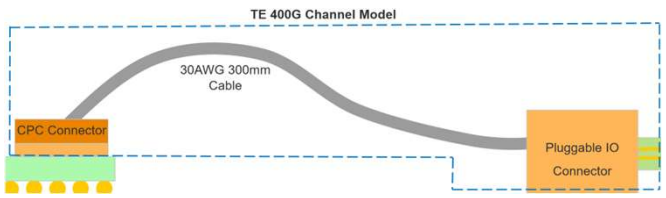
Insertion Loss
Return Loss
PowerSum Crosstalk

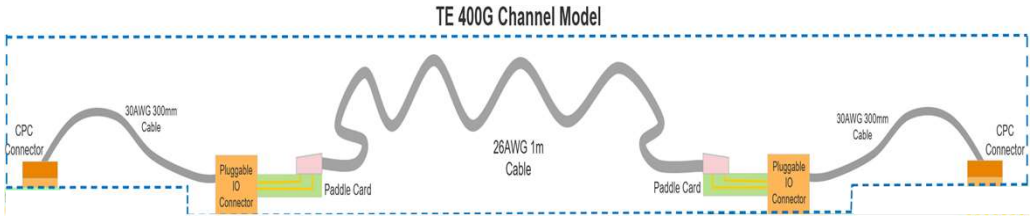
Crosstalk includes 5 FEXT, 3 NEXT

Models are preliminary and under development.

400 Gbps Imperatives

- Insertion Loss: PCB, Substrate trace loss is challenging at these candidate Nyquist frequencies and densities. Twinax cable-based architectures are a viable alternative.
- Return Loss: Relentless drive for optimized transitions to minimize reflections is critical. Interconnect mating interfaces and leadframes will be streamlined
- Crosstalk: Interconnect design and PCB/Substrate escapes will be highly shielded to minimize near and far end crosstalk. This is especially critical at the densities required.





Summary

- 400G+/lane parts start to ramp in 2028, driven by AI.
- Transition to 400G+/lane drives addressable challenges along all SI vectors: loss, crosstalk, reflections.
- Addressing the SI challenges in the accelerated adoption time frame demands an optimized approach to channel development.
- TE Connectivity is providing early simulation-based 448G VSR and LR channels.
- Face plate pluggable module and passive copper cable-based architectures are promising realities at 448 Gbps